Relay-Based Computing

Computer Architecture, Fall 2008

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Presenter ID 349, Poster #38

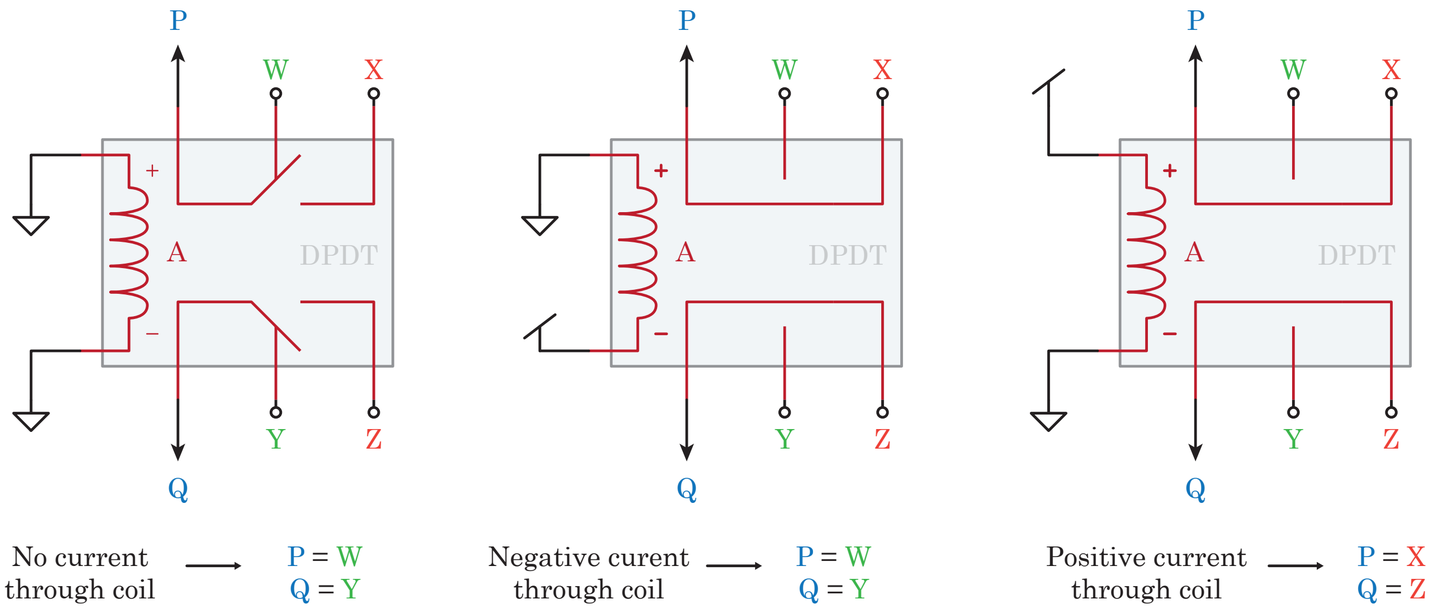
Phase 1 (December 2008)

8-bit relay-based ALU

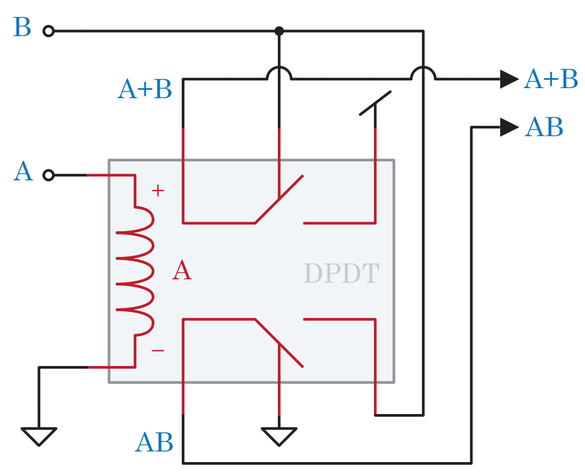
Add / Subtract / XOR

Microcontroller test unit

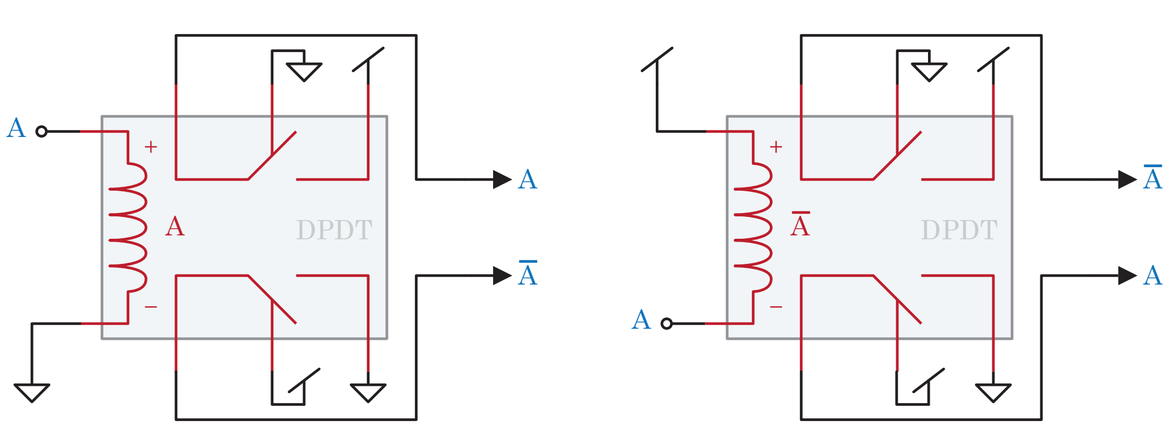
Polarized DPDT Relays



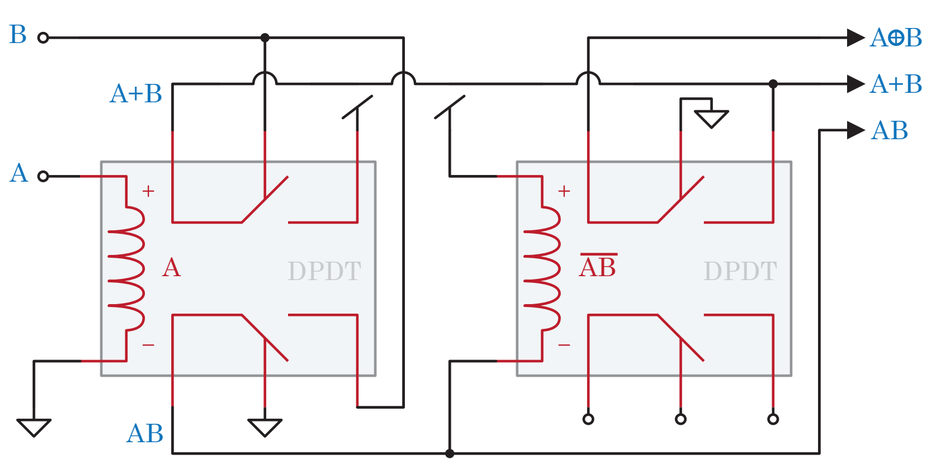
AO (AND/OR) Gate



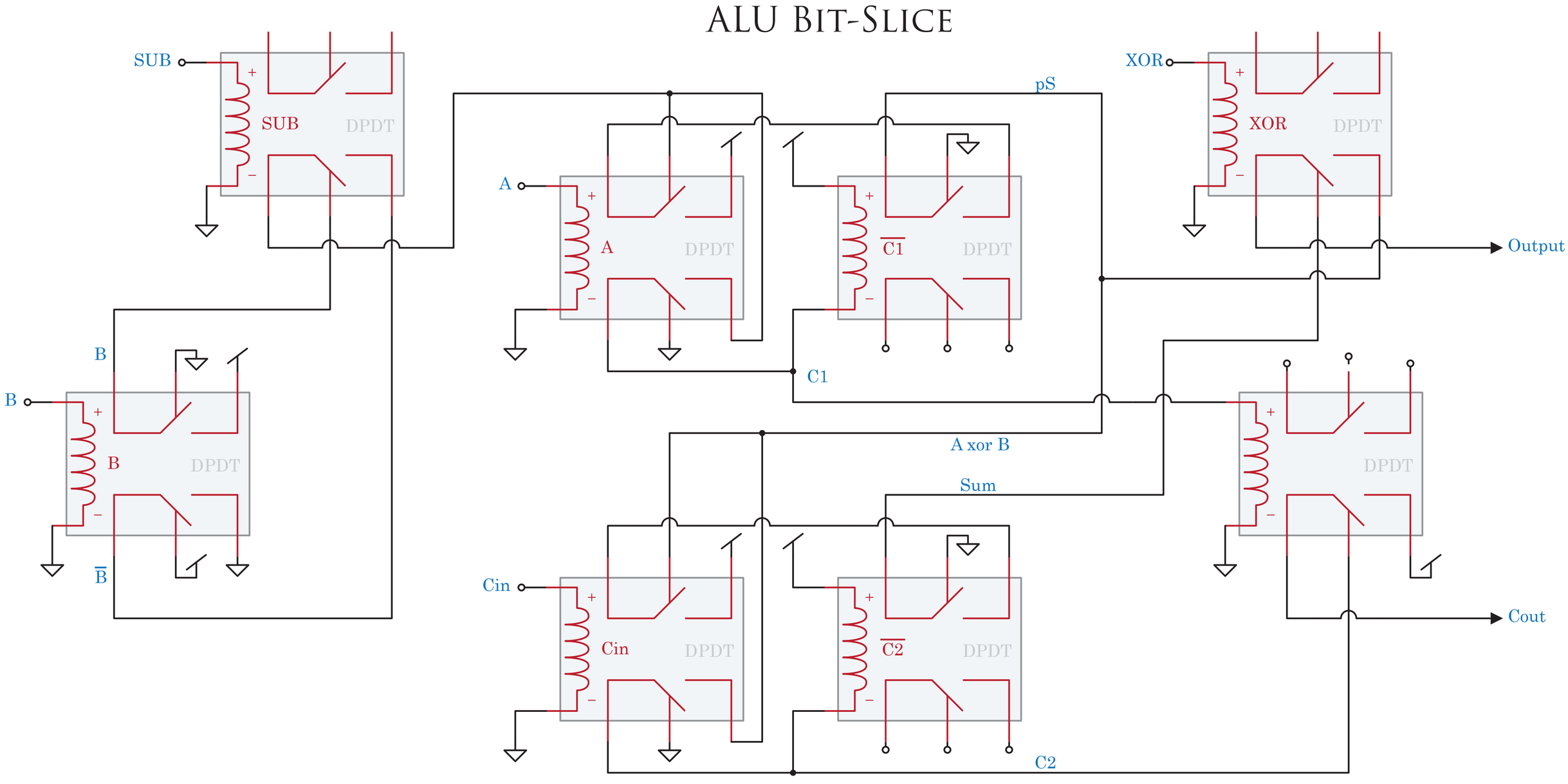
Buffers & Inverters



Two-Relay AOX (AND/OR/XOR) Gate



ALU Bit-Slice



Shared Mux-Relay Architecture (SMRA) --> Decrease relay count in each bit slice