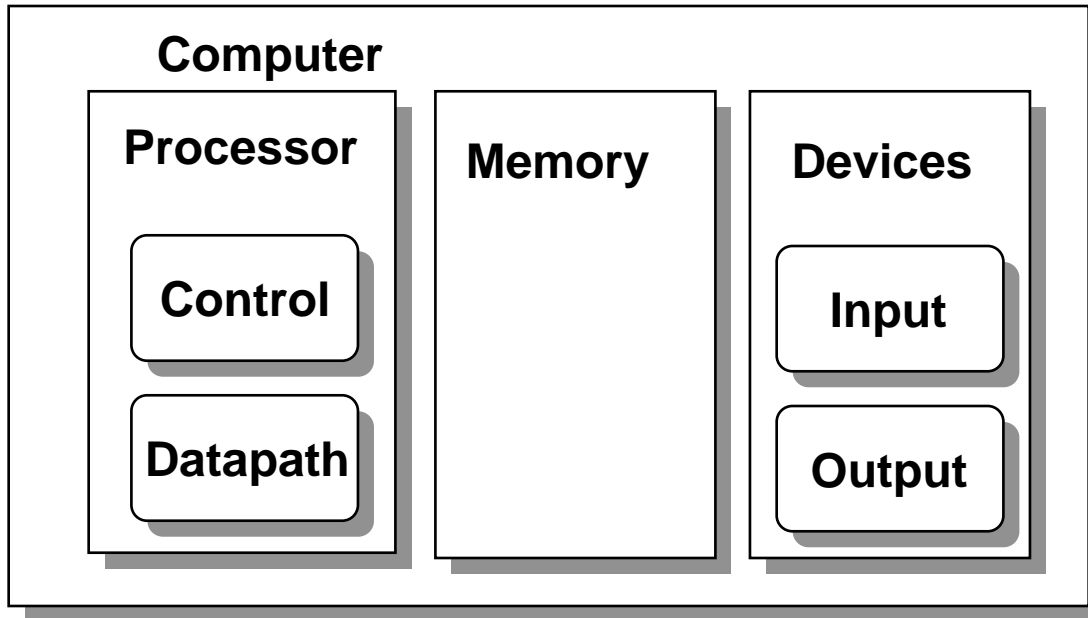


Datapath & Control

Readings 5.1-5.4



Datapath: System for performing operations on data, plus memory access.

Control: Control the datapath in response to instructions.

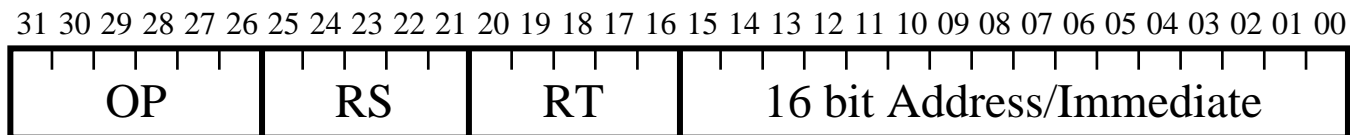
Simple CPU

Develop complete CPU for subset of instruction set

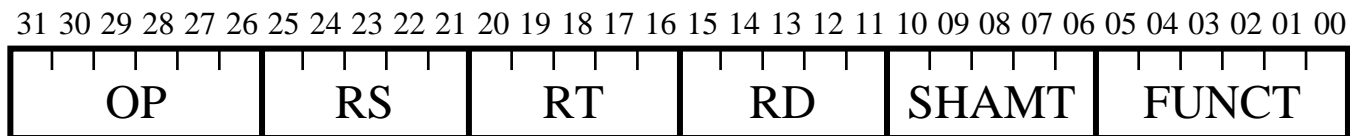
Memory: lw, sw

Branch: beq

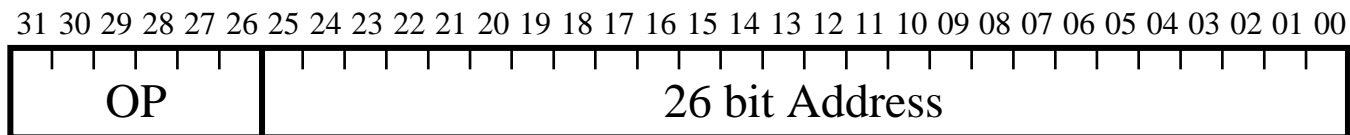
Arithmetic: addi



Arithmetic: add, sub

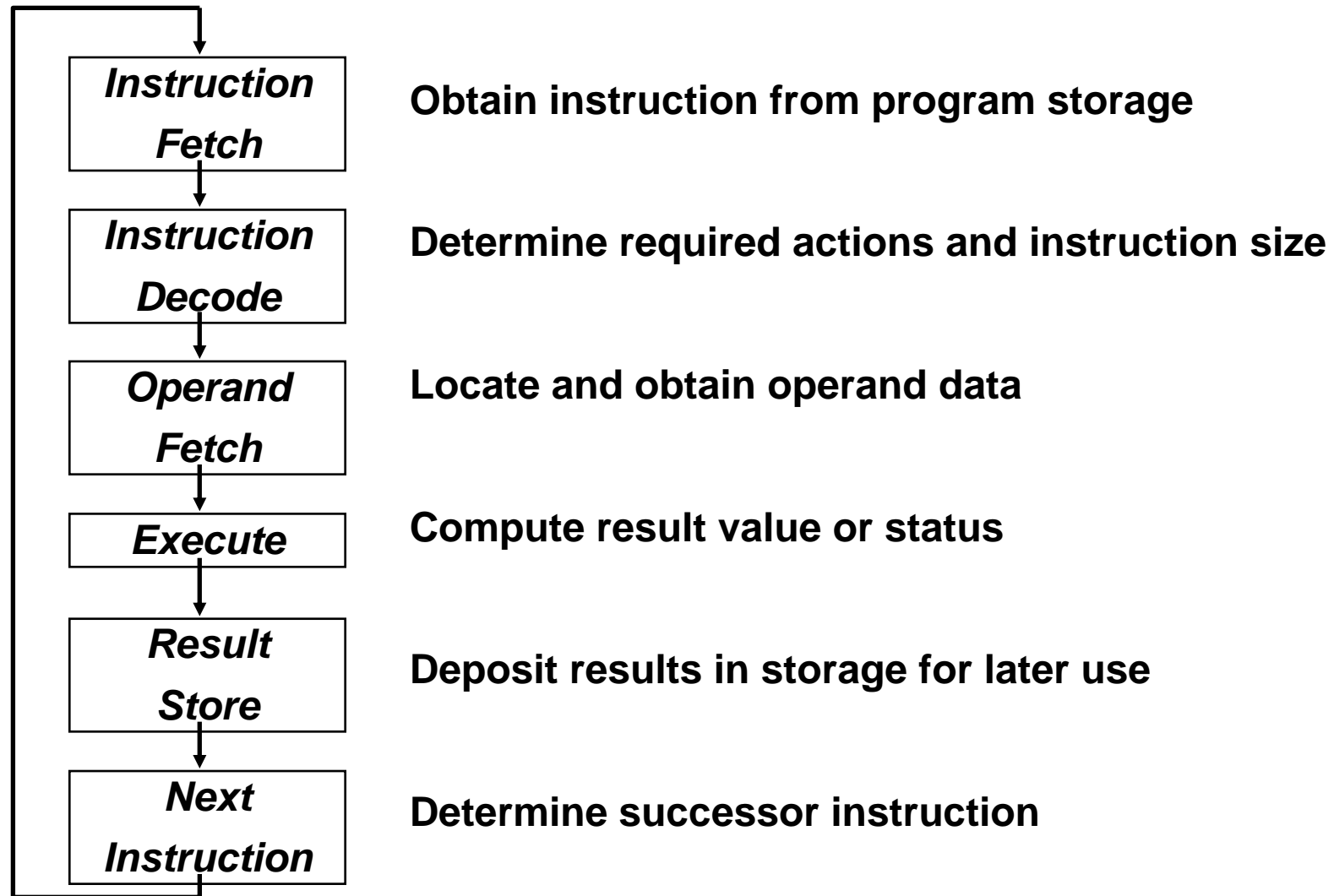


Jump: j



Most other instructions similar

Execution Cycle



Processor Overview

Overall Dataflow

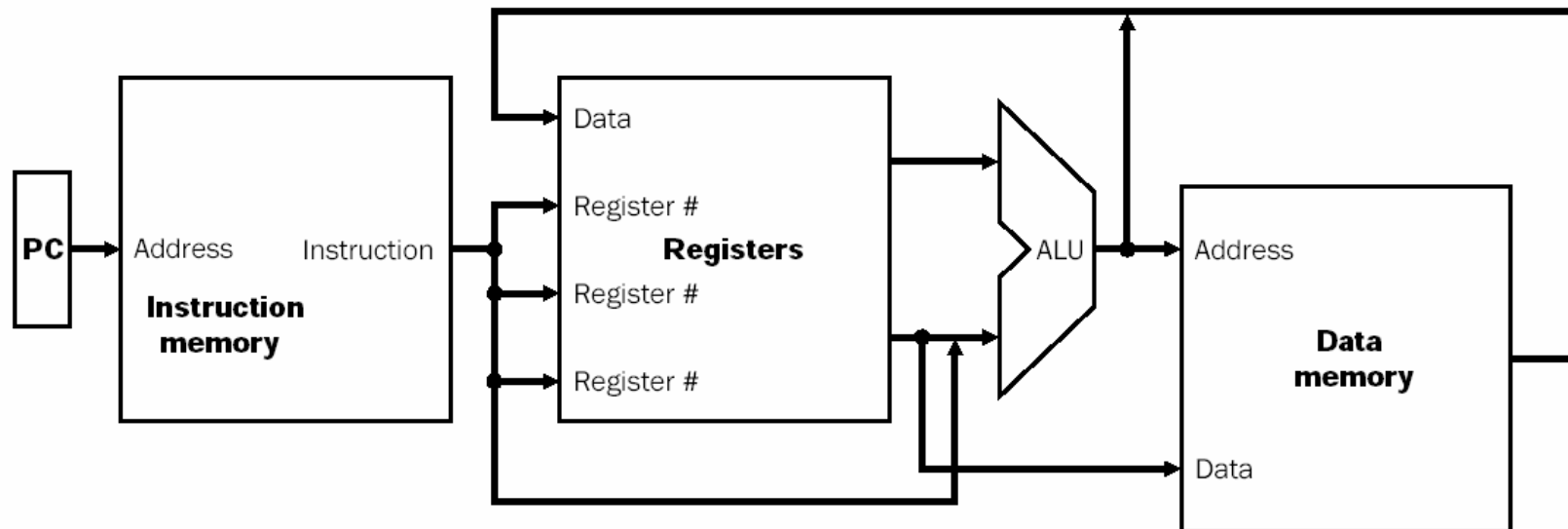
PC fetches instructions

Instructions select operand registers, ALU immediate values

ALU computes values

Load/Store addresses computed in ALU

Result goes to register file or Data memory



Processor Design

Convert instructions to Register Transfer Level (RTL) specification

$\text{Instruction} \leftarrow \text{Memory}[\text{PC}];$

$\text{PC} \leftarrow \text{PC} + 4;$

RTL specifies required interconnection of units

Control designed to achieve given paths for each instruction

Instruction Fetch UNIT

```
Instruction = Mem[PC];    // Fetch Instruction  
PC = PC + 4;             // Increment PC (32bit)
```



Add/Subtract RTL

Add instruction: add rd, rs, rt

Instruction = Mem[PC];

Reg[rd] = Reg[rs] + Reg[rt];

PC = PC + 4;

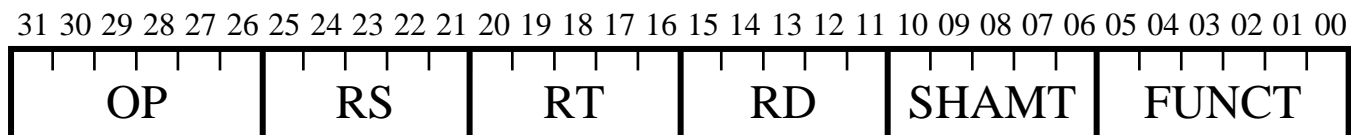
Just Feed

Subtract instruction: sub rd, rs, rt

Instruction = Mem[PC];

Reg[rd] = Reg[rs] - Reg[rt];

PC = PC + 4;



Datapath for Reg/Reg Ops

$\text{Reg}[\text{rd}] = \text{Reg}[\text{rs}] \text{ op } \text{Reg}[\text{rt}];$

Controls

**Instruction
Fetch
Unit**

Instructions[31:0]

[25:21]

[20:16]

[15:11]

Rs

Rt

Rd

Rd

Rs

Rt

ALUcntrl

Aw Aa Ab Da
Dw Db
Register
WrEn File

RegWr

*Control
Lines*

Regwr

ALUcntrl

op

Add Immediate RTL

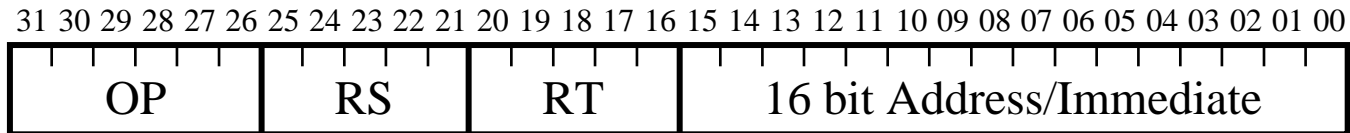
Add immediate instruction: `addi rt, rs, imm`

`Instruction = Mem[PC];`

`Reg[rt] = Reg[rs] + SignExtend(imm);`

`PC = PC + 4;`

Ifetch



Datapath + Immediate Ops

$\text{Reg}[\text{rt}] = \text{Reg}[\text{rs}] + \text{SignExtend}(\text{imm});$

