- How would the ALU be used to help with each of the following branches? The first is filled in for you:
  - beq (\$rs == \$rt) subtract \$rt from \$rs, use zero flag
  - \* bne (\$rs != \$rt) sub tri from \$rs, use ! zero \* bgez ( $\$rs \ge 0$ )  $\$rs \ddagger \$0$  ', ! negative flag \* bgtz (\$rs > 0)  $\$rs \ddagger \$0$  , ! neg AND ! zero.
  - Solution (srs > 0) dus fab, (he) dus fab, (he)
  - \* bltz (\$rs < 0) \$vs + \$0, neg flag.

Design a 4-bit sra (shift arithmetic right) unit. Note that sra \$t0, 1 = \$t0/2, \$t0, 2 = \$t0/4, ...  Write MIPS assembly to compute \$t1 = \$t0\*5 without using a multiply or divide instruction.

add  $J_{1}, J_{1}, J_{2}, J_{1}, J_{$ 

SII J+1, \$to12 (1+1= tox f add +1, to1+1

What is the value of the following floating-point number?

What is done for these ops during each of the CPU's execute steps at right? \* \* add \$t0, \$t1, \$t2 sw \$t3, 16[\$t4] lw \$t5, 8[\$t6] Get Instr-Instruction Fetch Figure out op Instruction Decode ber +1, t2 +3,+4 Operand 46 Fetch do add set from add mem[] -> +5 do adel do add Execute Jave to to \$13 -> MAMERAN Result Store Next CF VC+4 Instruction 14 Immediate vals for ADDI are sign-extended, while those for ORI are extended with zeros. Build a sign-extend unit that can handle both.



 Develop a single-cycle CPU that can do LW and SW (only). Make it as simple as possible

