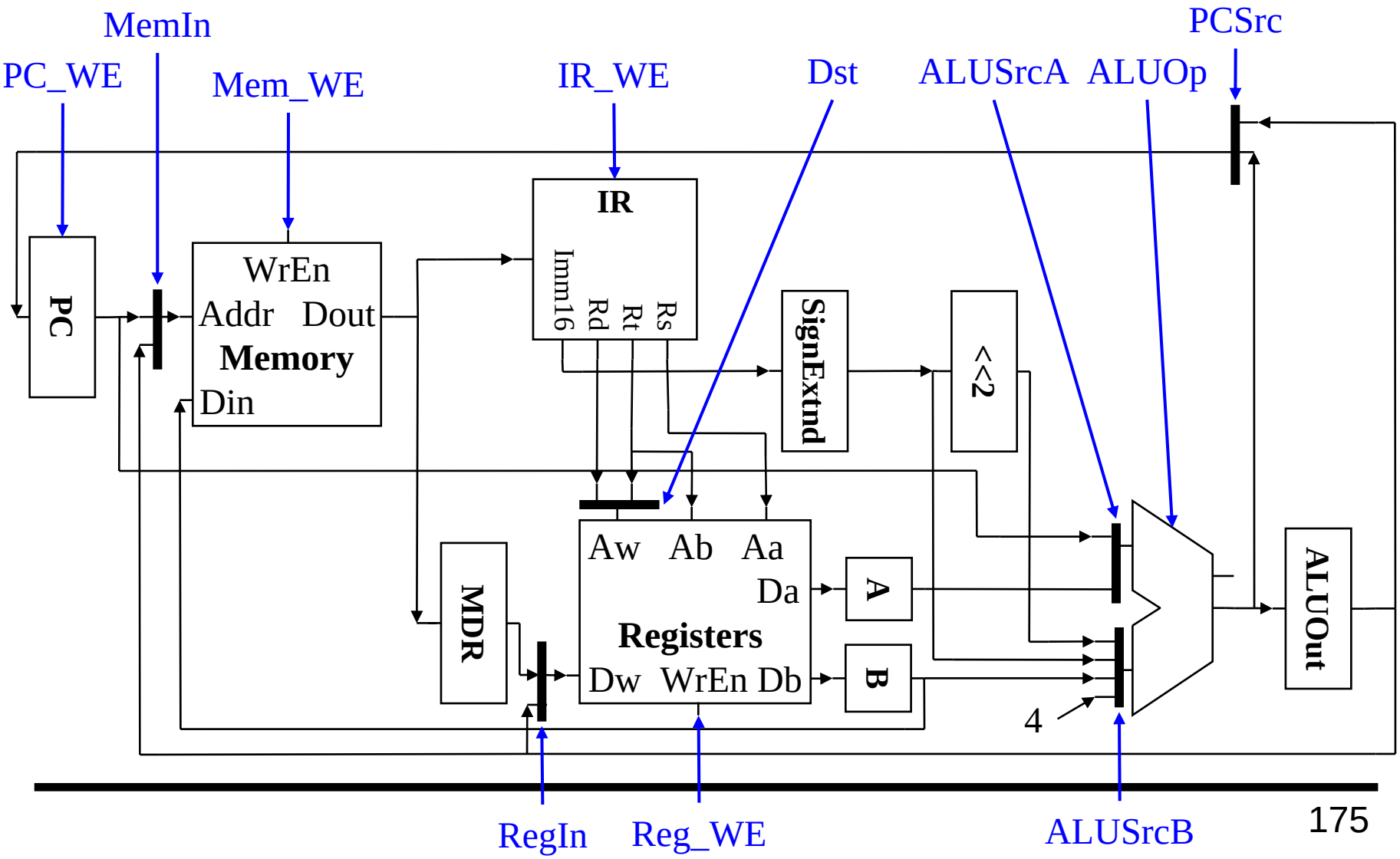
Datapath Control Signals



Multicycle Datapath Control

	WE				ALU						
State	PC	Mem	Reg	IR	SrcA	SrcB	Op	Dest	MemIn	RegIn	PCSrc
1	1	0	0	1	PC	4	+	X	PC	X	ALU
2	0	0	0	0	PC	<<2	+	X	X	X	X
3Br	(zero)	0	0	0	A	B	-	X	X	X	ALUout
3Rt	0	0	0	0	A	B	(IR)	X	X	X	X
4Rt	0	0	1	0	X	X	X	Rd	X	ALUout	X
3St	0	0	0	0	A	SE	+	X	X	X	X
4St	0	1	0	0	X	X	X	X	ALUout	X	X
3Lo	0	0	0	0	A	SE	+	X	X	X	X
4Lo	0	0	0	0	X	X	X	X	ALUout	X	X
5Lo	0	0	1	0	X	X	X	Rt	X	MDR	X
					A	<<2		Rt[20:16]	PC	MDR	ALU
					PC	SE		Rd[15:11]	ALUout	ALUout	ALUout
						B					
						4					

```
1:
IR = Mem[PC]
PC = PC + 4

2:
A = Reg[Rs]
B = Reg[Rt]
ALUOut = PC
  + (SE(imm16)<<2)

3Br:
Zero = (A-B)
If (zero) PC = ALUout

3Rt:
ALUout = A op B

4Rt:
Reg[Rd] = ALUout

3St:
ALUout = A + SE(Imm16)

4St:
Mem[ALUout] = B

3Lo:
ALUout = A + SE(Imm16)

4Lo:
MDR = Mem[ALUout]

5Lo:
Reg[Rt] = MDR
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