ENGR 3410: Lab #0
CPU Building Blocks

Due: September 29, 2005, beginning of class

The purpose of this lab is to develop some basic building blocks for your pseudo-MIPS processor and further refine your skills with Verilog and Verilog simulation. My time estimate is 3-6 hours.

Construct the following circuits, consulting Appendix B as necessary:

- 2:1 (two-input) multiplexor
- 4:1 (four-input) multiplexor
- 2-bit decoder
- 2-bit decoder with an enable

All logic must be gate level and structural. You only have the basic gates, such as AND, OR, NOT, NAND, NOR, XOR. No assign statements (except to set a wire to a constant value), registers, case statements, etcetera. All of these basic gates must have a delay of 50 time units.

On the due date, hand in your Verilog code, your test bench, and the appropriate simulation output (simulation results in text or waveform) for each circuit. Electronic submissions are welcome, and should be copied to both myself and Mike Curtis. We prefer a single, well-named archive file (ZIP or TAR) containing a directory with all your files. For instance, if you are *Team Smack*, your directory would be "teamsmack", and you would ZIP that up into a file "teamsmack.zip".

Due to the simplicity of this lab, we will not be performing demos. You may turn in one deliverable for all group members.

We expect all group members to participate in every aspect of this lab.

You would do well to read the Verilog tutorial I provide on the class wiki.