ENGR 3410: HW#1
Digital Logic

Due: September 22, 2006

The purpose of this homework is to hone your digital logic skills and to introduce you to Verilog and our Verilog simulation environment. Please show all your work.

1.1

An equality circuit is one whose output is true when both inputs are the same. Show all three forms: Boolean equation, truth table, and circuit. Use only the basic gates, AND, OR, NOT, NAND, NOR.

1.2

Simplify the following Boolean equations:

$f_1 = AB + AC + \bar{A}B$

$f_2 = (AD + \bar{A}C)[\bar{B}(C + B\bar{D})]$

1.3

Draw the schematics (circuits) for the following functions using NOR gates and inverters only.

$\left[\overline{\overline{X} + (\overline{Y + Z})}\right]$

$\overline{\left[\overline{(\overline{\overline{X} + \overline{Y}})} + \overline{(\overline{X} + \overline{Z})}\right]}$

1.4

Form the complement of the following functions:

$f_3 = [A + \overline{BCD}][\overline{AD} + B(\overline{C} + A)]$

$f_4 = A\bar{B}C + (\bar{A} + B + D)(AB\bar{D} + \bar{B})$

1.5

Construct a truth table and schematic for and XOR gate using only AND, OR, and NOT gates.

1.6

Construct and simulate a two-input XOR gate in Verilog using only these basic gates: AND, OR, NOT. You must demonstrate that your circuit works. Hand in your Verilog code, your test bench, and the appropriate simulation output (simulation results in text or waveform). You would do well to read the Verilog tutorial I provide on the class wiki.