ENGR 3410: HW#3
Single Cycle Processor
Diagnostic Homework

October 6, 2006

The purpose of this homework is to probe your understanding of MIPS single-cycle processor design. This homework will not be graded, however, I will take a peek at it if you like, before the midterm exam. The solutions are posted on the class wiki.

3.1 Optimization

You have a friend, let's call him Joe Optimal. He wants to eliminate the control signal `MemToReg` from the single cycle processor designed in class. You talk to Joe, and realize that he isn't suggesting that we remove the multiplexor entirely. Is this possible? Why or why not?

3.2 Extending our instruction set

Take the single cycle processor developed in class, and add the instructions below. Show the changes to the single-cycle datapath (including the instruction fetch) needed to support all these instructions, as well as the ones done in class. Show the control signal settings needed for each of these instructions.

- `BNE`
- `LW_R $dest, $addr, $addr2`
  (The RTL for this instruction is `Reg[$rt] = Mem[$rs + $rt]`)
- `WAI`
  (The *where am I* instruction. The RTL is `Reg[$rt] = PC`)

3.3 Swapping

In our single-cycle processor design (as-is), can we implement the swap instruction as described in Exercise 2.59 (P&H and on the wiki) without modifying the register file? Explain.