

ENGR 3410: MP#0

CPU Building Blocks

Due: October 2, 2007, 5pm

The purpose of this machine problem is to develop some basic building blocks for your pseudo-MIPS processor and further refine your skills with Verilog and Verilog simulation. You will also be getting to know your team members in this machine problem. My time estimate is 3-6 hours.

0.1 The Problem

Construct the following circuits, consulting Appendix B as necessary:

- 2:1 (two-input) multiplexor
- 4:1 (four-input) multiplexor
- 2-bit decoder
- 2-bit decoder with an enable

All logic must be gate level and structural. You only have the basic gates, such as AND, OR, NOT, NAND, NOR, XOR. No assign statements (except to set a wire to a constant value), registers, case statements, etcetera. All of these basic gates must have a delay of 50 time units.

You will likely want to check out the digital logic book in reserve to get firm definitions of multiplexors and decoders. Also, as mentioned above, check out Appendix B! You may use any sources you like, but make sure that it agrees with what is described in our textbook.

0.2 Turn-in Requirements

I expect a semi-formal, electronic, “lab write-up” of this machine problem. It does not need to be as rigorous as lab notebooks in other, more experimental classes. It should include, at a minimum:

- A brief write-up of the experiments
- Files of all Verilog code — modules and test benches

- Simulation output (textual or waveform) for each circuit

We would prefer this packaged as a single document (Word, L^AT_EX, PDF) and supporting Verilog code, in a single, well-named archive file (ZIP or TAR). Please name this file after your team. So if you are *Team Smack*, your directory would be “teasmack”, and you would ZIP that up into a file “teasmack.zip”.

Other notes:

- You may turn in one deliverable for all group members
- Please email your documents to myself and John Morgan
- We expect all group members to participate in every aspect of this lab
- You would do well to read the Verilog tutorial I provide on the class wiki