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Digital Design

ENGR 3410 - Computer Architecture

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Combinational Logic Design Process

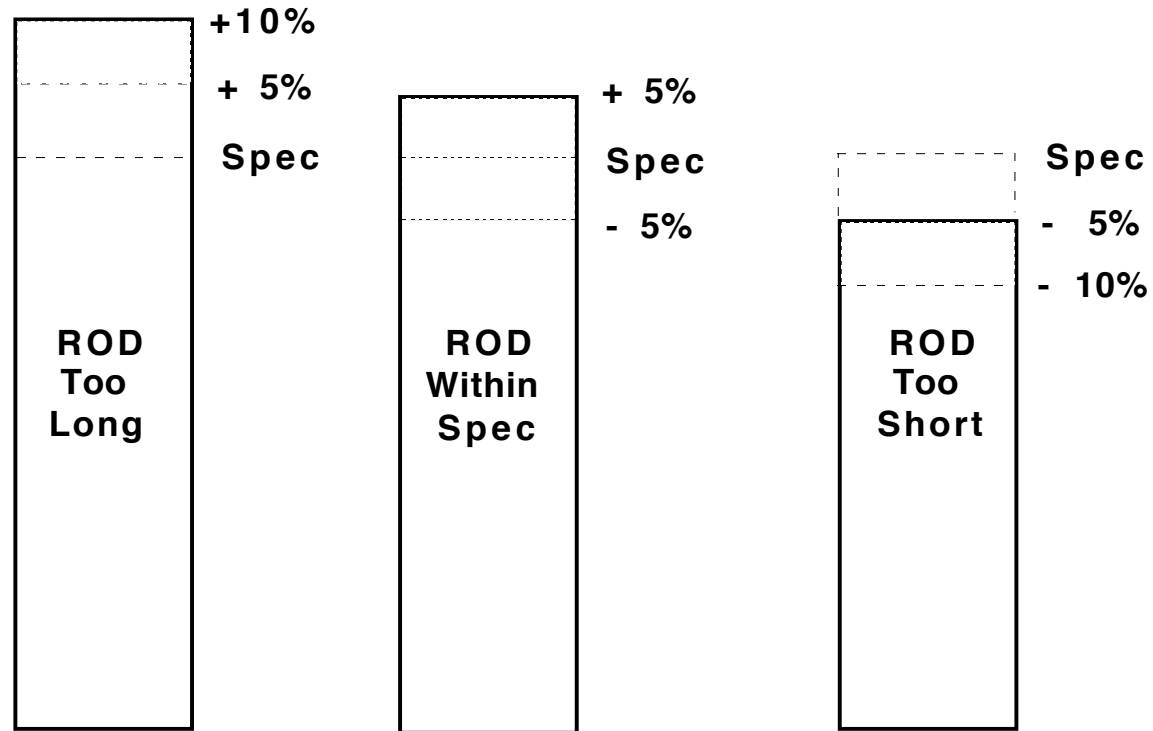
- Understand the Problem
 - what is the circuit supposed to do?
 - write down inputs (data, control) and outputs
 - draw block diagram or other picture
- Formulate the Problem in terms of a truth table or other suitable design representation
 - truth table, Boolean algebra, etc.
- Choose Implementation Target
 - PAL, PLA, Mux, Decoder, Discrete Gates
- Follow Implementation Procedure
 - K-maps, Boolean algebra, algorithmic simplification

Process Line Control Example

- Statement of the Problem
 - Rods of varying length (+/-10%) travel on conveyor belt
 - Mechanical arm pushes rods within spec (+/-5%) to one side
 - Second arm pushes rods too long to other side
 - Rods too short stay on belt

 - 3 light barriers (light source + photocell) as sensors
 - *Design combinational logic to activate the arms*
- Understanding the Problem
 - Inputs are three sensors, outputs are two arm control signals
 - Assume sensor reads "1" when tripped, "0" otherwise
 - Call sensors A, B, C
- Draw a picture!

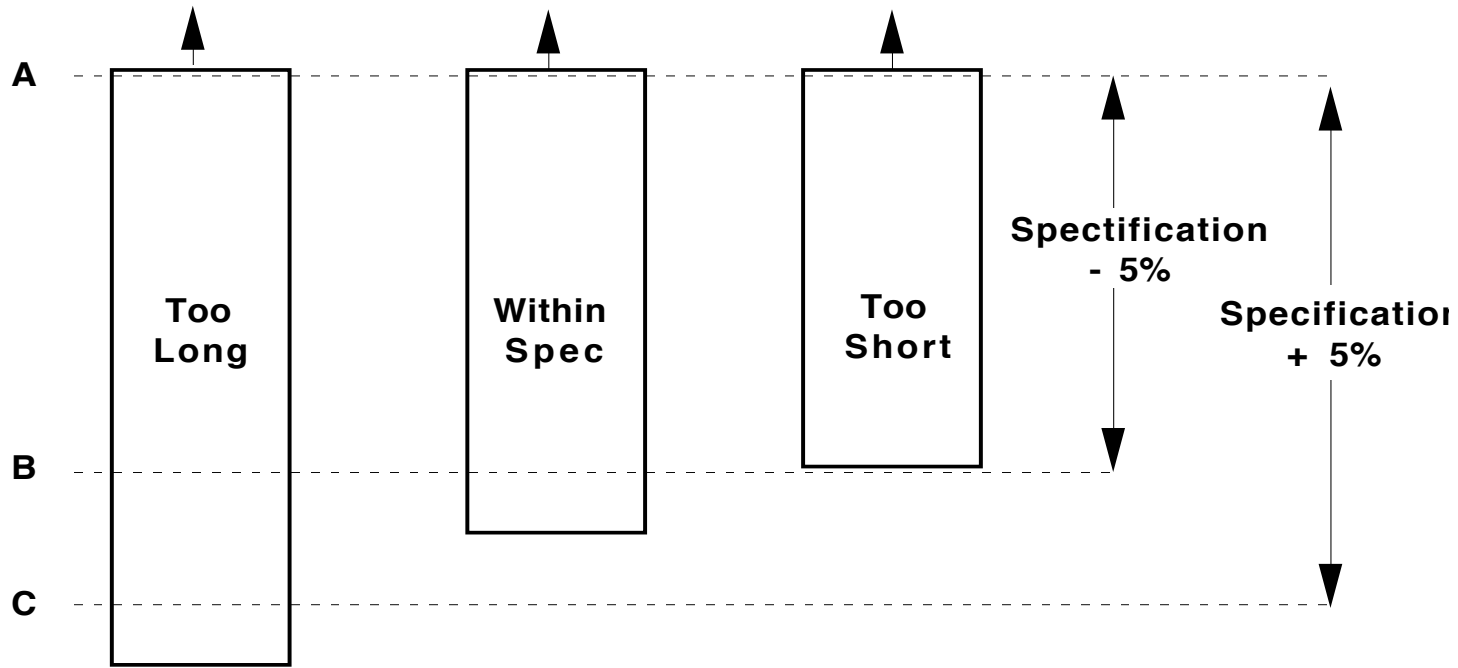
Process Line Control Example (cont.)



Where to place the light sensors A, B, and C to distinguish among the three cases?

Assume that A detects the leading edge of the rod on the conveyor

Process Line Control Example (cont.)

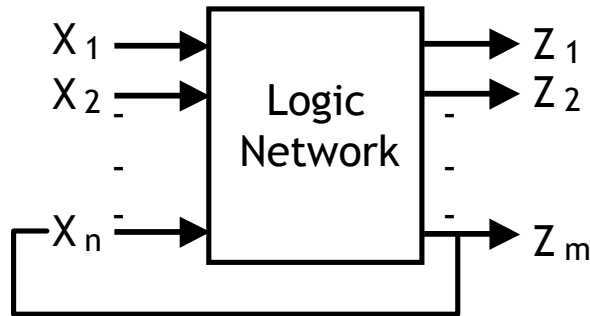


A to B distance placed apart at specification - 5%

A to C distance placed apart at specification +5%

Process Line Control Example (cont.)

Combinational vs. Sequential Logic



Network implemented from logic gates.
The presence of feedback distinguishes between *sequential* and *combinational* networks.

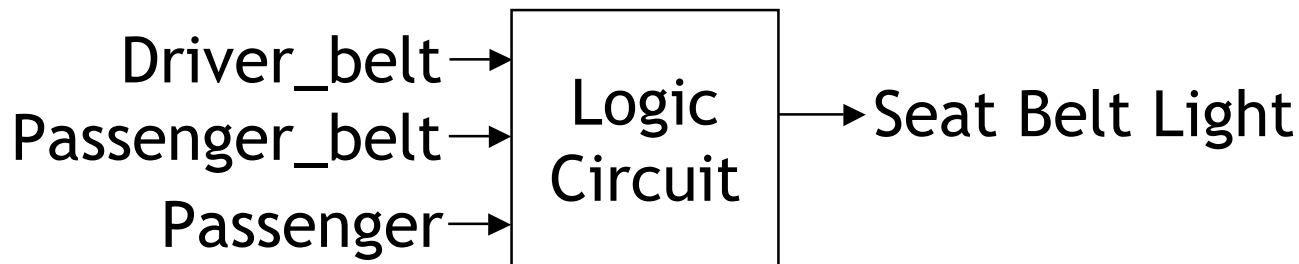
Combinational logic

no feedback among inputs and outputs

outputs are a pure function of the inputs

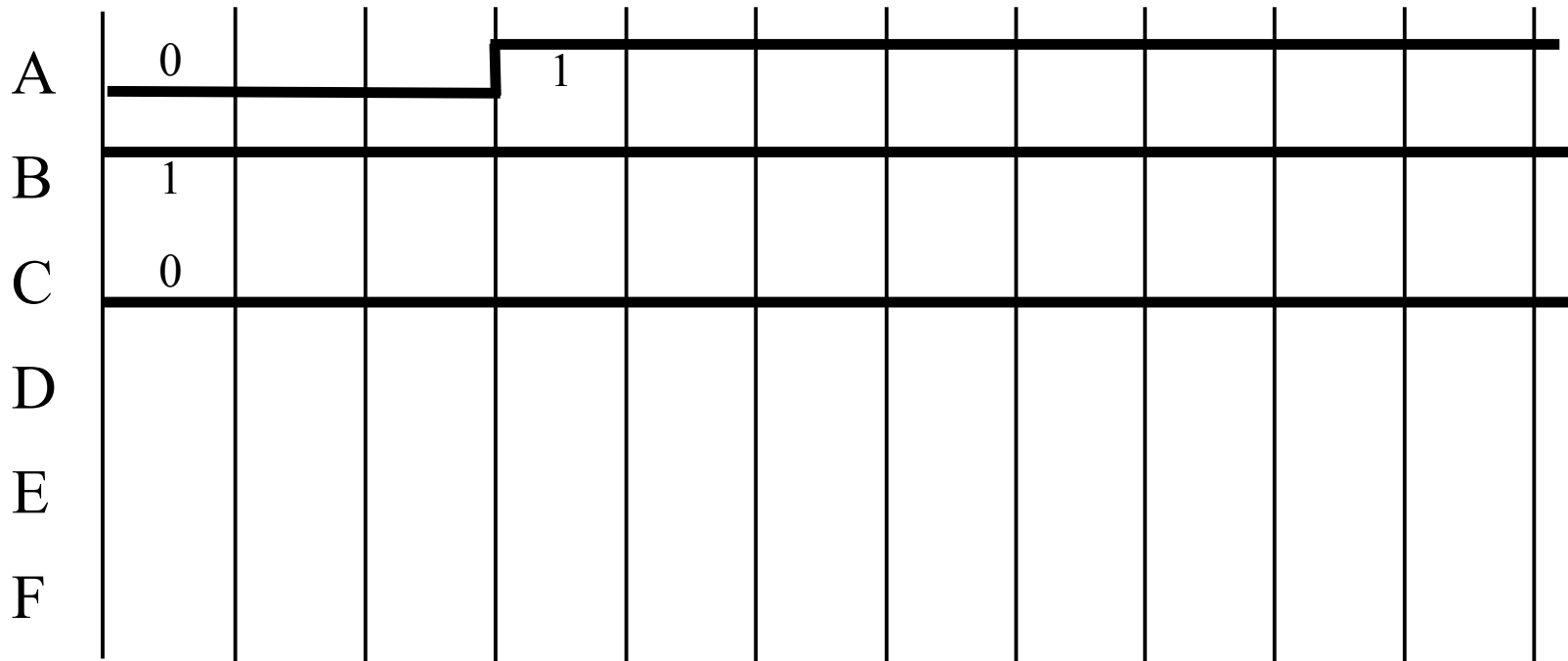
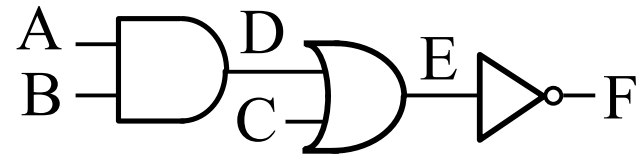
e.g., seat belt light:

(Dbelt, Pbelt, Passenger) mapped into (Light)



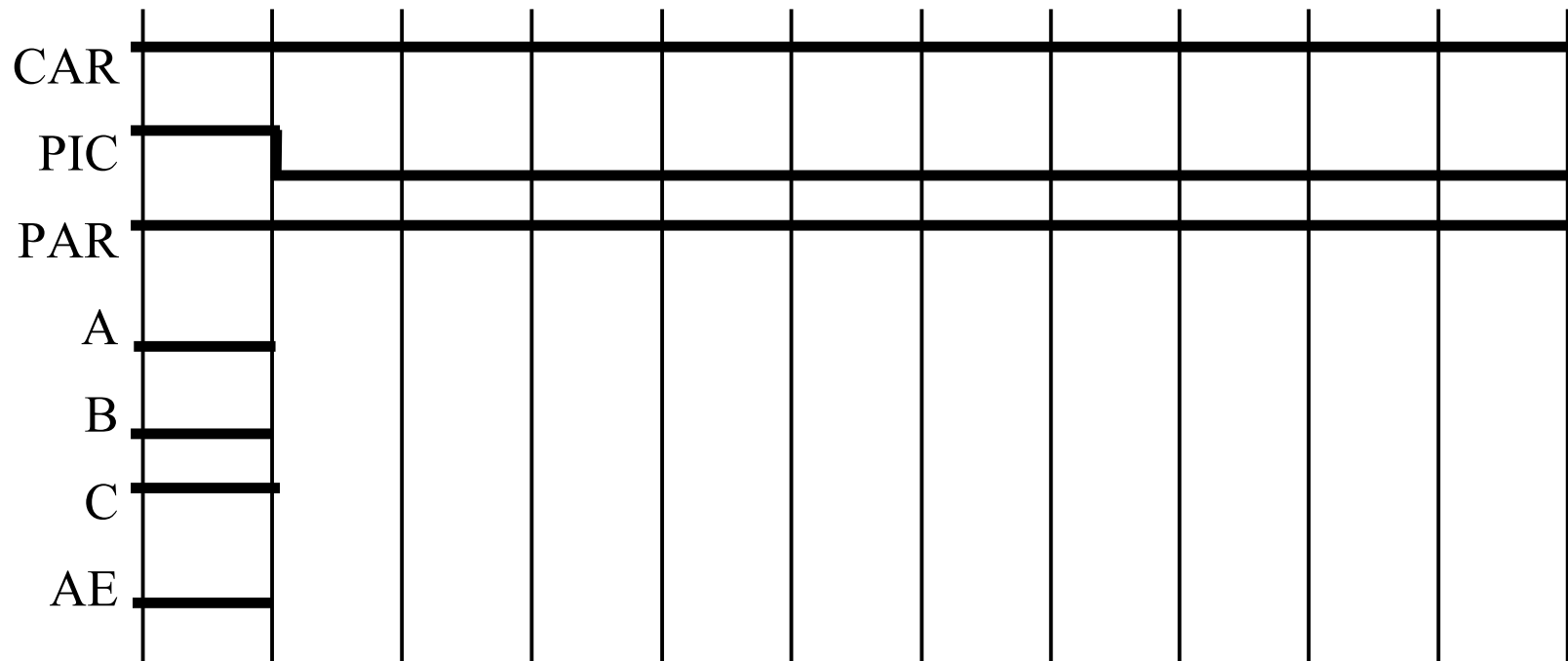
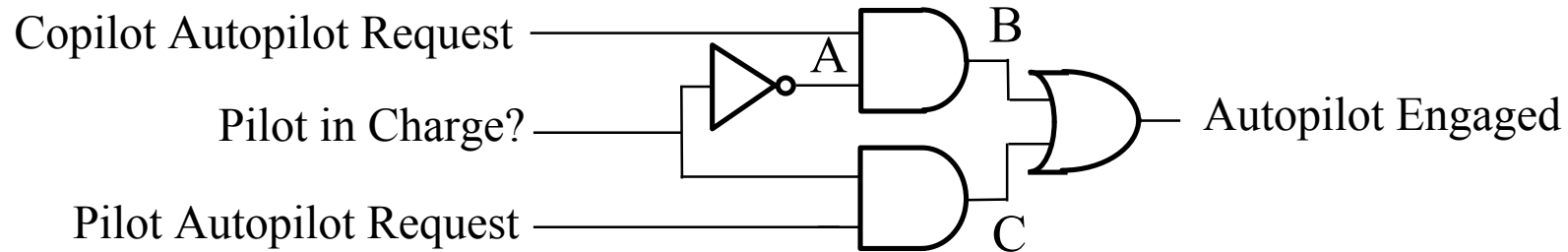
Circuit Timing Behavior

- Simple model: gates react after fixed delay



Hazards/Glitches

- Circuit can temporarily go to incorrect states



- Must filter out temporary states

Safe Sequential Circuits

- Clocked elements on feedback, perhaps outputs
 - Clock signal synchronizes operation
 - Clocked elements hide glitches/hazards

