

## Cadence Verilog Simulation Tutorial

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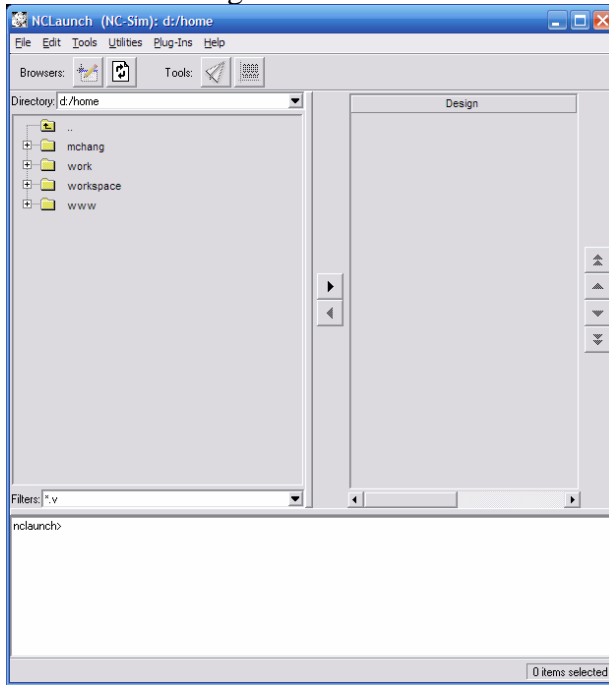
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Cadence version: Cadence IUS 05.41-s011

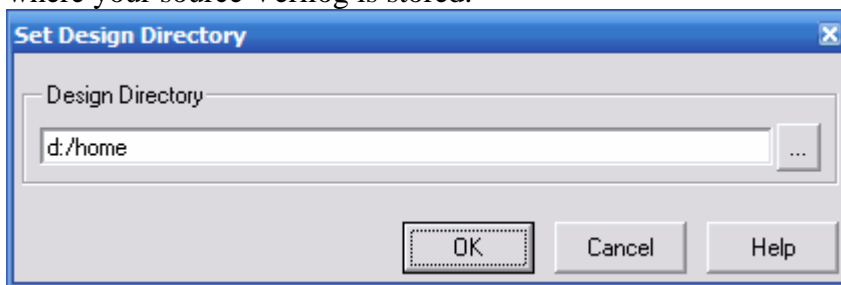
This tutorial was originally written for ENGR 3410, Computer Architecture. It may apply to any course using the Olin-licensed Cadence IUS/LDV simulation tools.

- 1) Install Cadence IUS as per the IT instructions (can be found on our wiki or on the IT web site). That means install Cadence IUS by running **setup.exe** from the following directory:  
[\\stuapp\NETAPPS\Cadence\IUS54QSR2\\_wint.Update\CDROM1\Setup.exe](\\stuapp\NETAPPS\Cadence\IUS54QSR2_wint.Update\CDROM1\Setup.exe)
  - a. You will be installing the IUS tools. You *will not* be installing the license manager. *Uninstall all previous versions of the IUS tools first.*
  - b. Follow all obvious prompts and install the obvious/defaults. I have already installed this software at the time of this tutorial, so I do not have screenshots. Sorry.
  - c. The license manager should already be set if you have installed other Cadence software (for instance, PSPICE). If not, the license manager should be set to **5280@STUAPP**.
  - d. Restart if instructed.
  - e. The Cadence IUS tools are now in your Start Menu under *Cadence Design Systems*.

- 2) This tutorial assumes you have some Verilog to simulate. We will present the example of the first lab in ENGR 3410, which is a MIPS register file. Organize your Verilog source and tests into one directory and start the program called *NCLaunch*. If asked, choose single-step simulation. You should then be presented with the following window:

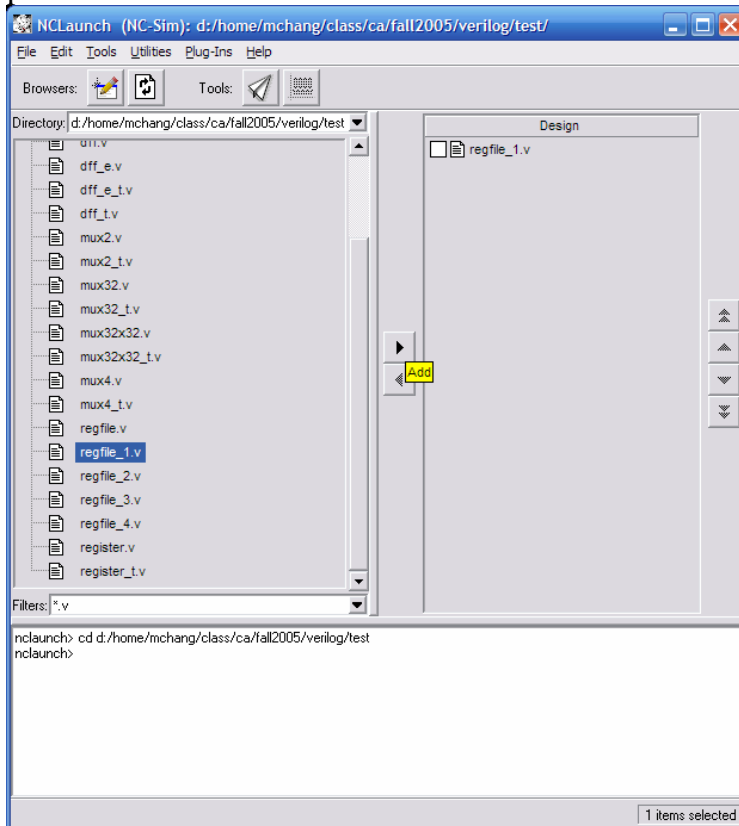


- 3) Select File > Set Design Directory  
4) From the pop-up window, select the “...” for the design directory and navigate to where your source Verilog is stored.

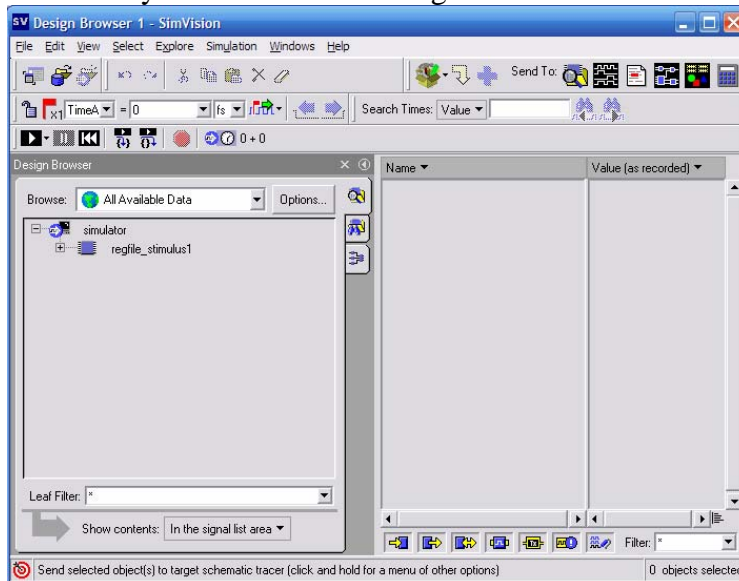


- Now, you will see all your files in the left pane.  
5) Now, choose the Verilog test bench file that you want to simulate and click the right arrow button in the center of the window to move that file to the “Design”

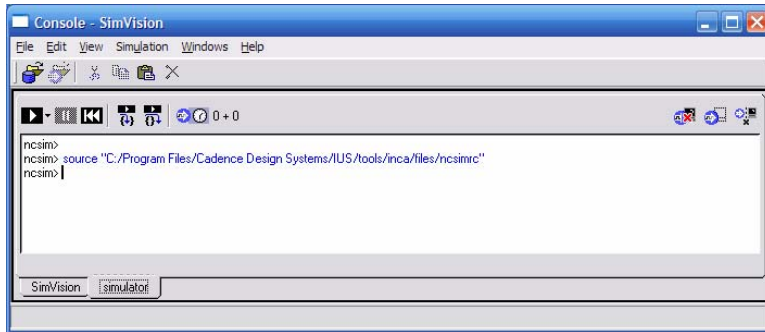
panel.



- 6) Now, on the right, select the file you want to simulate. *Do not check the check box. I have no idea what that check box does.* And then click the paper airplane icon in the toolbar.
- 7) SimVision should launch when you press the paper airplane icon. The default window layout consists of a Design Browser window:

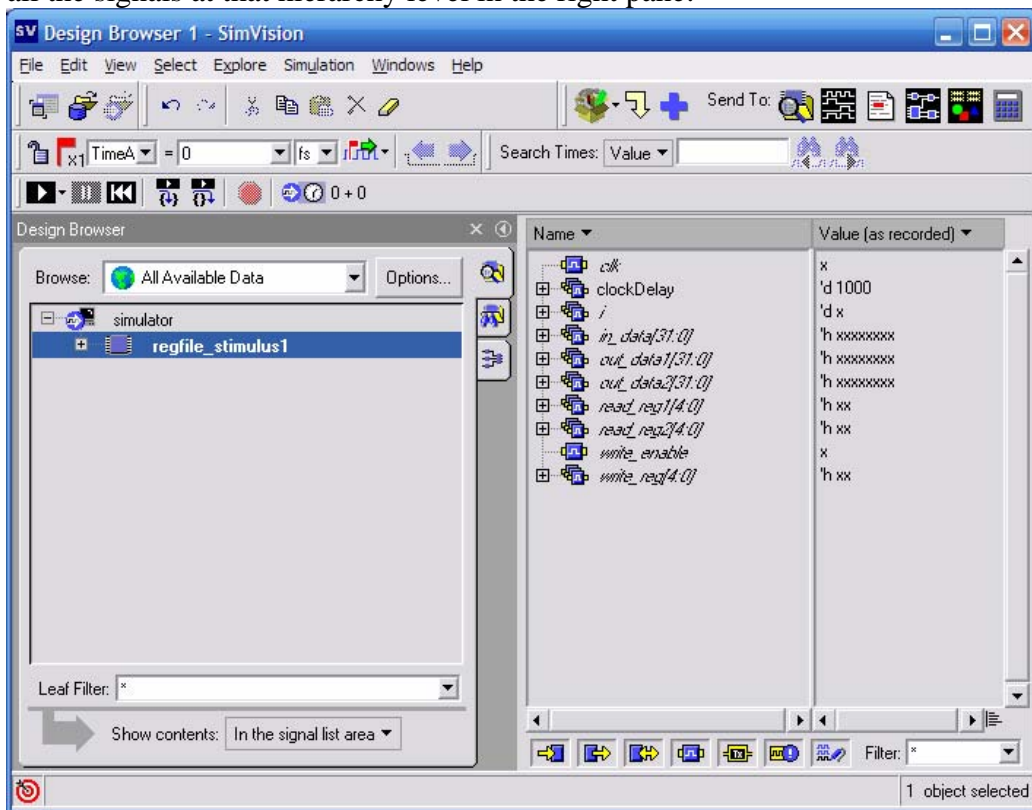


and a Console window:

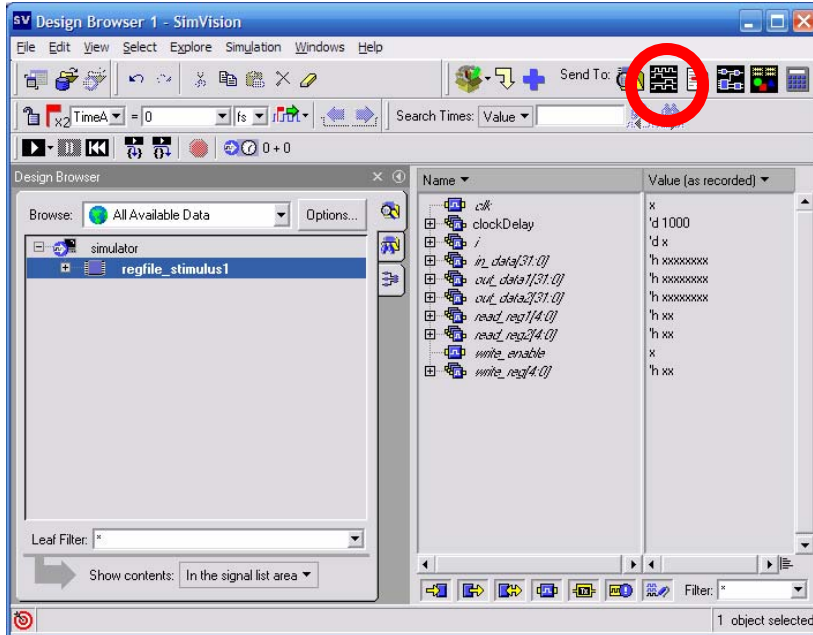


We will be working mostly with the Design Browser window.

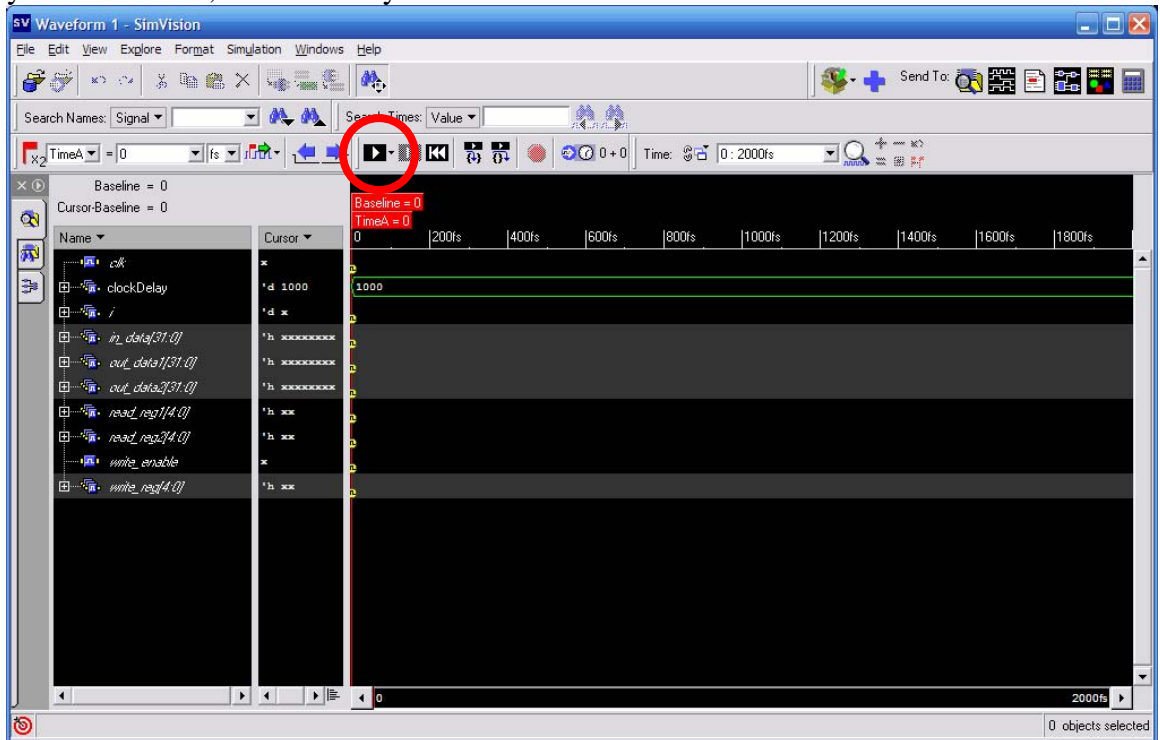
- 8) In the Design Browser window, you will see a hierarchical representation of your module in the left pane. Clicking on the first (highest-level) module will display all the signals at that hierarchy level in the right pane:



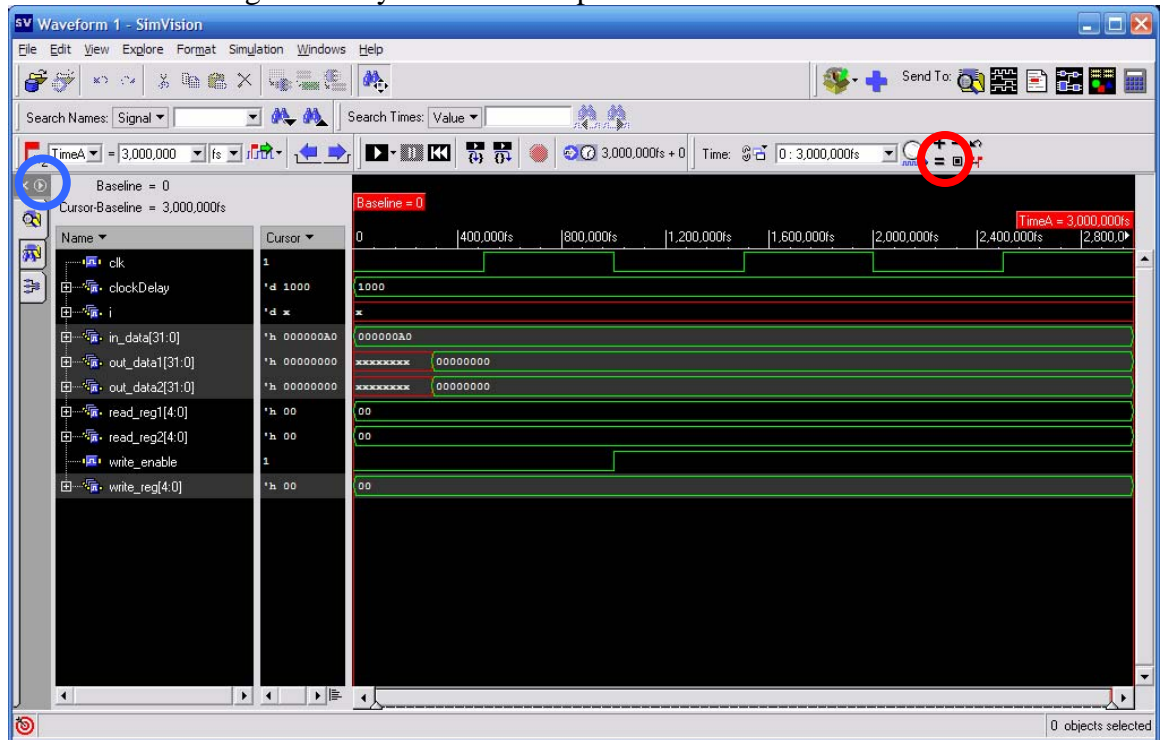
- 9) To add all these signals to the waveform viewer, click on the “Send To: Waveform window” button:



- 10) This will open the Waveform viewer that looks like the screenshot below. To run your simulation, click the Play button.



- 11) The Play button runs your simulation to the \$finish statement. It could take some time. Keep an eye on your processor load. When it is finished, you should see traces for all the signals that you selected to probe:



- The signal window will just be zoomed in at the very beginning, and likely you'll want to zoom out. To zoom out to see *everything*, click on the magnifying glass with an equals sign in it (highlighted above).
- To add signal probes into lower levels of hierarchy, simply click on the arrow marked in blue above. This opens a pane with the module hierarchy.
- Here you can select modules down in the hierarchy, and pick signals to watch. When you click on signals in the lower left-hand pane, they immediately go to the waveform window.

- 12) Unfortunately, these signals were probably not monitored during the initial simulation. You must reset the simulation and re-run it to collect these values. To do that, simply click on the rewind button next to the play button, and then begin the simulation again.
- 13) If you make a change to your design, you will need to reinvoke the simulator. To do so, select Simulation > Reinvoke Simulator. This should re-compile the dependent code you changed, re-elaborate the necessary modules, and reinvoke the simulator on the new snapshot.
- 14) Notes:
  - a. If you ask the simulator to simulate a lot of low-level signals, it will take *forever*. Your CPU will hit 100% utilization, and the simulation will seem to lock up. In those cases, I have usually just forcibly quit the application from the Windows Task Manager and restarted the simulation with a more selective set of signals.
  - b. Sometimes reinvoking the simulator does not work right. It has thrown various errors when it doesn't work, none of which seem logical. If all else fails, I simply start over.
  - c. Often, processes will start that lock the design directory even after all Cadence programs seem to be closed. Most likely there is a process oBserver.exe running that needs to be killed to free the directory lock.
  - d. You must be connected to the Olin network in order to use the Cadence simulation tools. The license server is a network machine (STUAPP) and must be reachable. This works reliably over VPN.
- 15) All of this can be done from the command line as well.
  - a. Execute `ncverilog <filename>` to do a text-only simulation.
  - b. Execute `ncverilog +gui <filename>` to do a GUI simulation.