ENGR 3410: MP#0
CPU Building Blocks

Due: Before Class September 28, 2009

The purpose of this machine problem is to develop some basic building blocks for your pseudo-MIPS processor and further refine your skills with Verilog and Verilog simulation. You will also be getting to know your team members in this machine problem. My time estimate is 3-6 hours per person.

0.1 The Problem

Construct the following circuits, consulting any outside sources as necessary. (A good one would be one of the appendices of your textbook!) You must define, in text the operation of the following circuits in addition to actually simulating them.

- 2:1 (two-input) multiplexor
- 4:1 (four-input) multiplexor
- 2-bit decoder
- 2-bit decoder with an enable

All logic must be gate level and structural. That means no higher-level Verilog constructs, such as IF, WHILE, or FOR loops. You only have the basic gates, such as AND, OR, NOT, NAND, NOR, XOR. No assign statements (except to set a wire to a constant value), registers, case statements, et cetera. All of these basic gates must have a delay of 50 time units.

You will likely want to check out the digital logic book in reserve to get firm definitions of multiplexors and decoders. Also, as mentioned above, check out Appendix B!

0.2 Turn-in Requirements

I expect a semi-formal, electronic, "lab write-up" of this machine problem. It does not need to be as rigorous as lab notebooks in other, more experimental classes. It should include, at a minimum:

- A brief write-up of the experiments
- Files of all Verilog code — modules and test benches
- Simulation output (textual or waveform) for each circuit

Please package your writeup (Word, LaTeX, PDF) and supporting Verilog code, in a single, well-named archive file (ZIP or TAR). Please name this file after your team. So if you are *Team Smack*, your directory would be "teamsmack", and you would ZIP that up into a file "teamsmack.zip".

Other notes:

- You may turn in one deliverable for all group members
- Please email your documents just to me
- We expect all group members to participate in every aspect of this lab
- You would do well to read the Verilog tutorial I provide on the class wiki