ENGR 3410: HW #1
Digital Logic and a bit of Verilog

Due: 20 September 2010

The purpose of this homework is to hone your digital logic skills and to introduce you to Verilog and our Verilog simulation environment. Please show all your work.

Honor Code Policy

You are to do this homework primarily alone. If you get stuck, you may consult anyone you like ***after*** *you have given the problem some serious effort. You must annotate, per problem, with any collaborators you had for that problem. Your aide should* ***not*** *simply provide you an answer to work backwards from: they are a resource, not an answer key. If you have any questions regarding resources, ask early, ask often.*

1.1

An equality circuit is one whose output is true when both inputs are the same. Show all three forms: boolean equation, truth table, and circuit. Use only the basic gates, AND, OR, NOT, NAND, NOR.

1.2

Simplify the following Boolean equations:

$f_1 = AB + AC + \bar{A}B$

$f_2 = (AD + \bar{A}C)[\bar{B}(C + B\bar{D})]$

1.3

Draw the schematics (circuits) for the following functions using NOR gates and inverters only.

$$\left[\overline{\overline{X} + (\overline{Y + Z})}\right]$$

$$\overline{\left[\overline{(\overline{X} + \overline{Y})} + \overline{(\overline{X} + \overline{Z})}\right]}$$

1.4

Form the complement of the following functions:

$$f_3 = [A + \overline{BCD}][\overline{AD} + B(\overline{C} + A)]$$

$$f_4 = A\bar{B}C + (\bar{A} + B + D)(AB\bar{D} + \bar{B})$$

1.5

Construct a truth table and schematic for an XOR gate using only AND, OR, and NOT gates.

1.6

Construct and simulate a two-input XOR gate in Verilog using only these basic gates: AND, OR, NOT.

You must demonstrate that your circuit works completely. Hand in your Verilog code, your test bench, and the appropriate simulation output (simulation results in text or waveform).

Your code should be commented. Your simulation results should be accompanied by a few words that describe how your simulation proves your XOR works.

You should use ModelSim. You would do well to read the Verilog tutorial available on the class wiki.