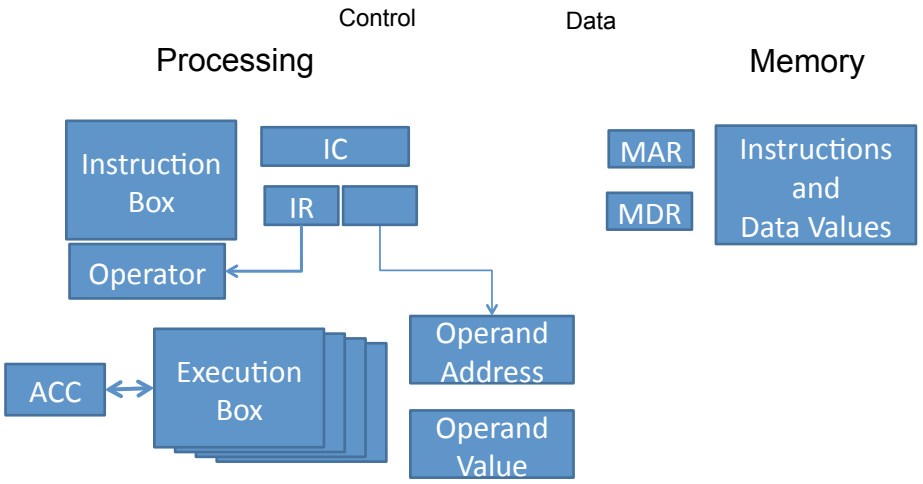
Computer Organization
Von Neumann Architecture

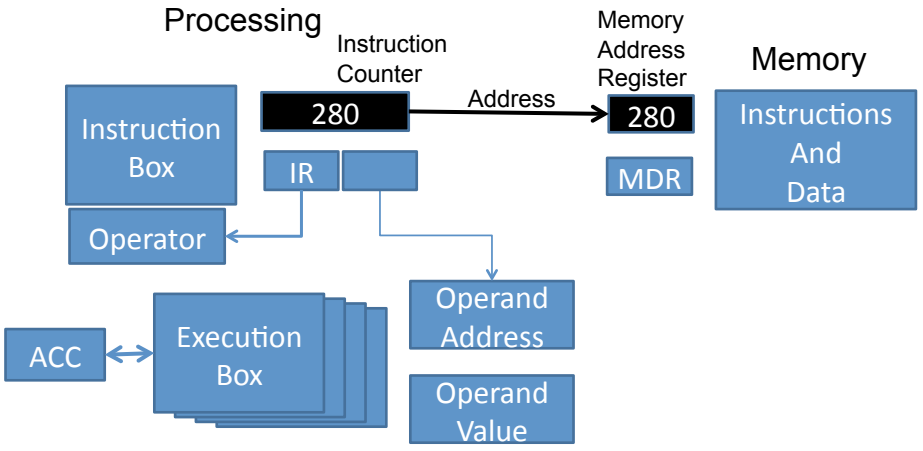
ENGR 3410 – Computer Architecture
Mark Sheldon
Alex Morrow
Fall 2010

Von Neumann Architecture

Von Neumann Architecture



Von Neumann Architecture
Instruction Fetch



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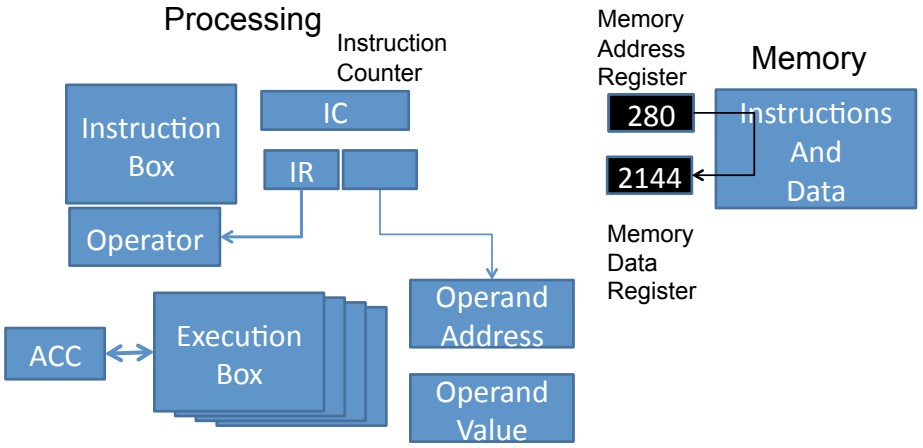

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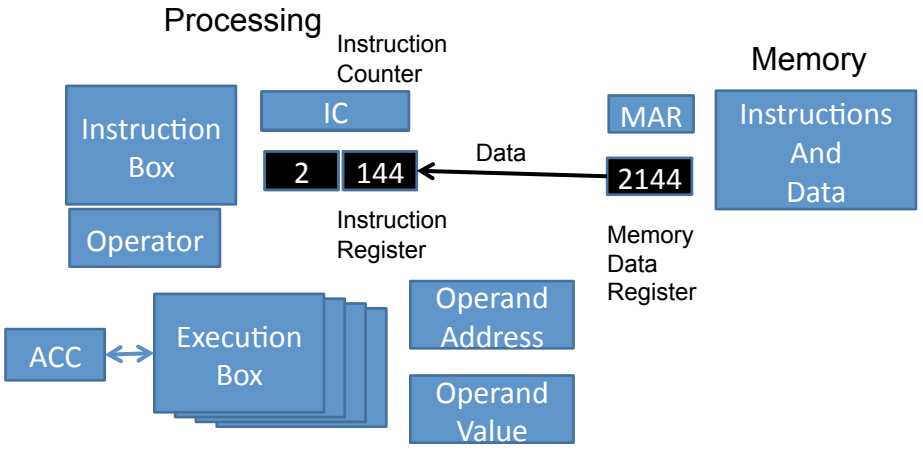
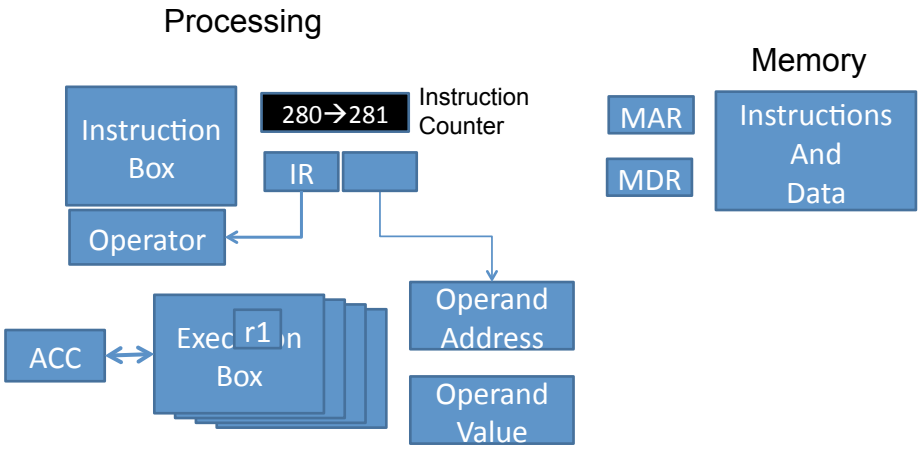
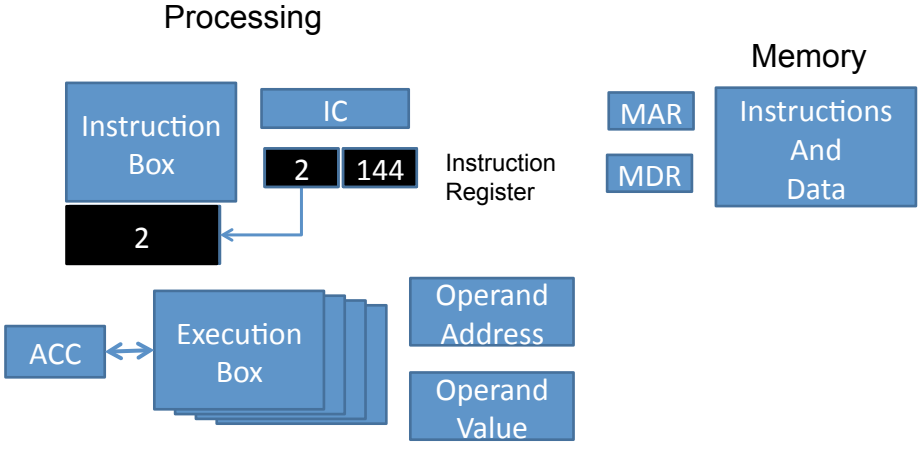


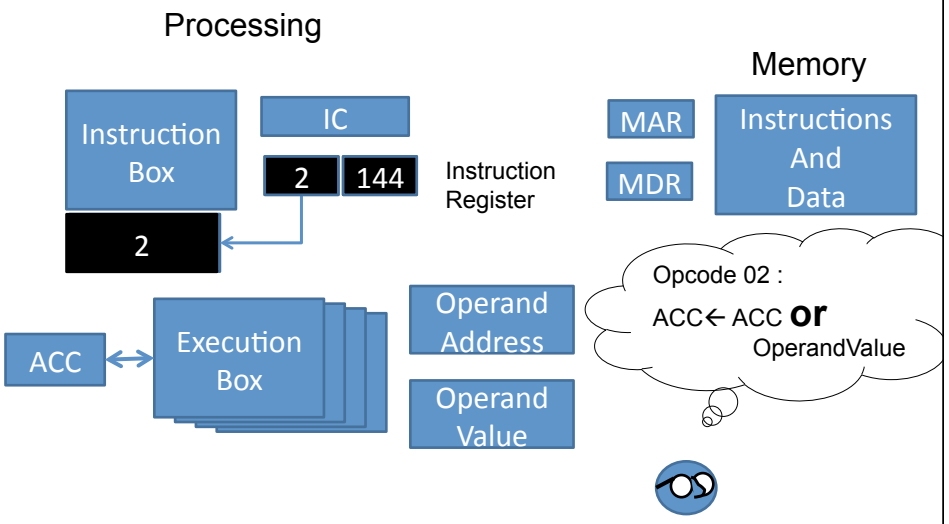
Von Neumann Architecture
Update Instruction Counter



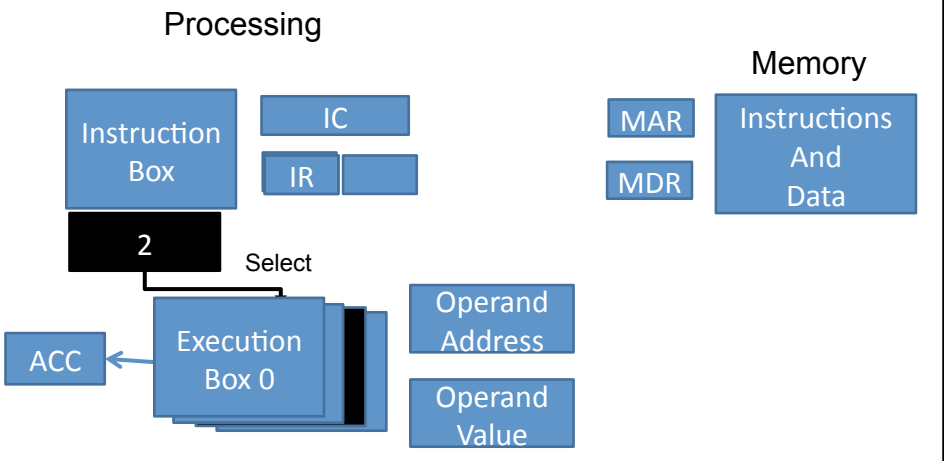
Von Neumann Architecture
Instruction Decode



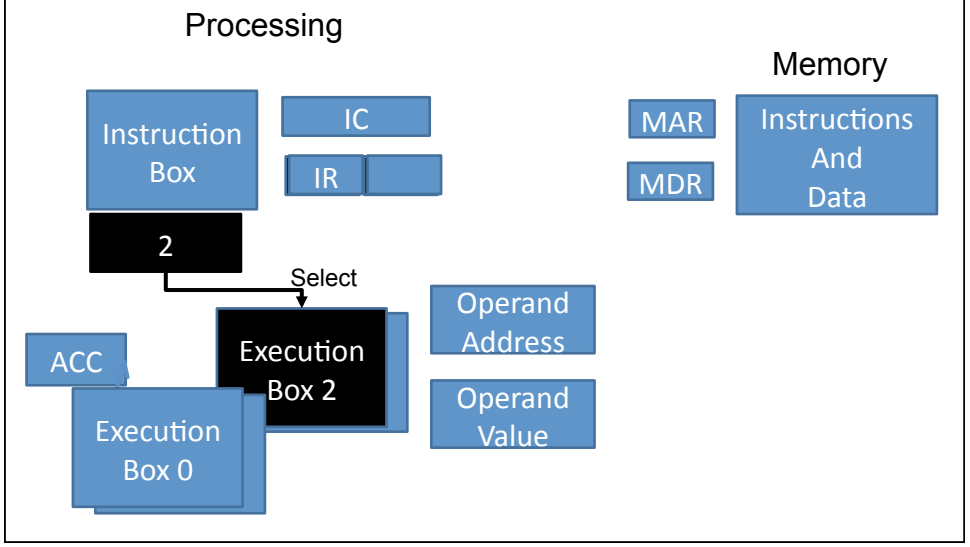
Von Neumann Architecture
Instruction Decode



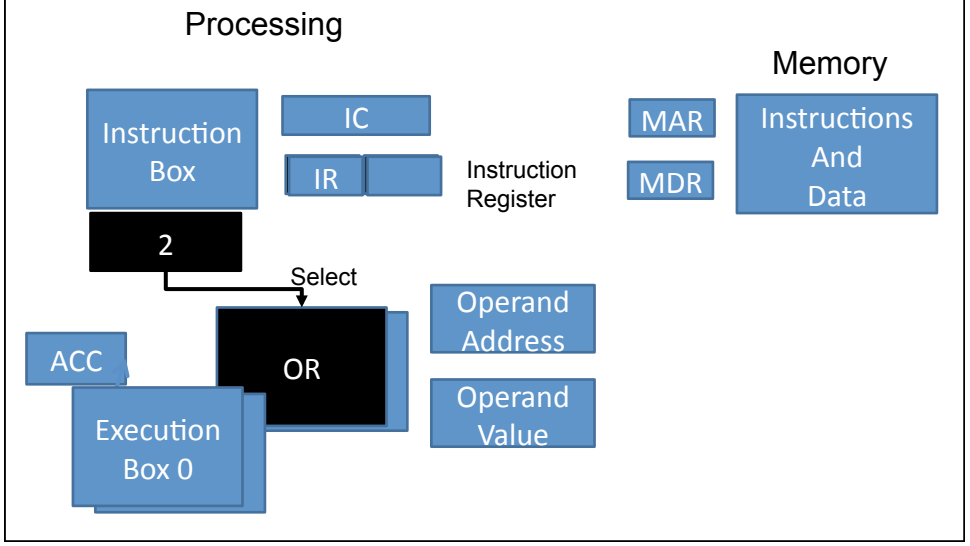
Von Neumann Architecture
Instruction Decode – Op Code



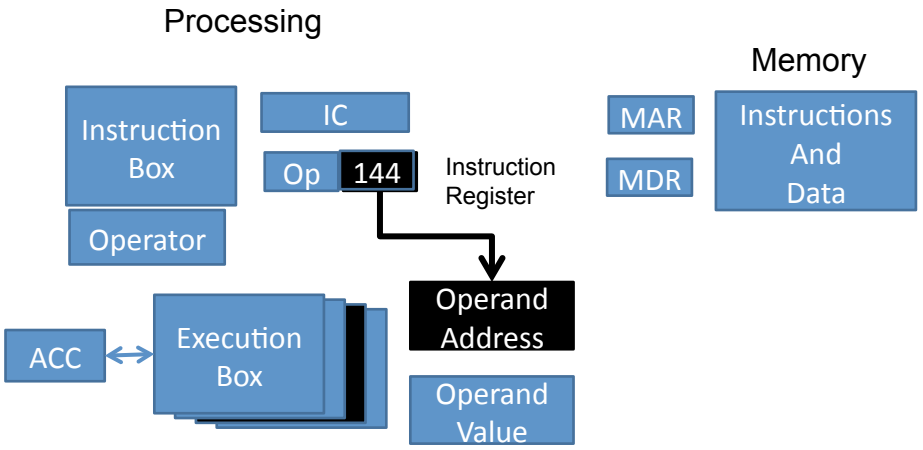
Von Neumann Architecture
Instruction Decode – Op Code



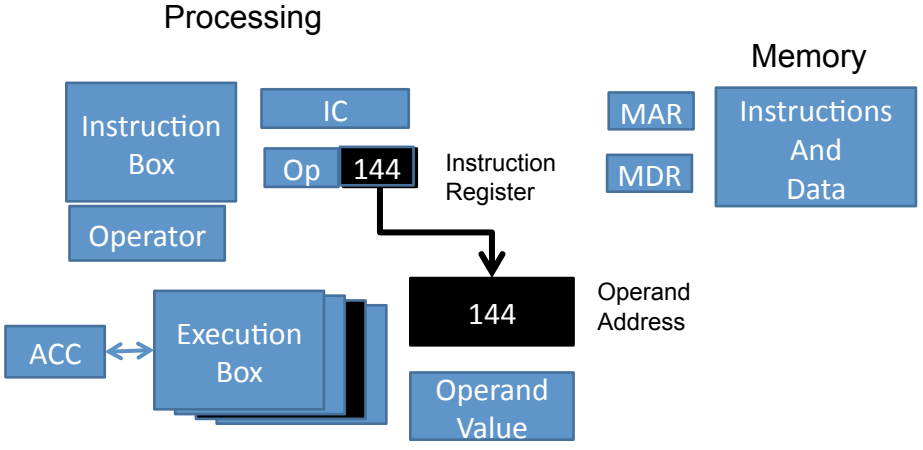
Von Neumann Architecture
Instruction Decode – Op Code



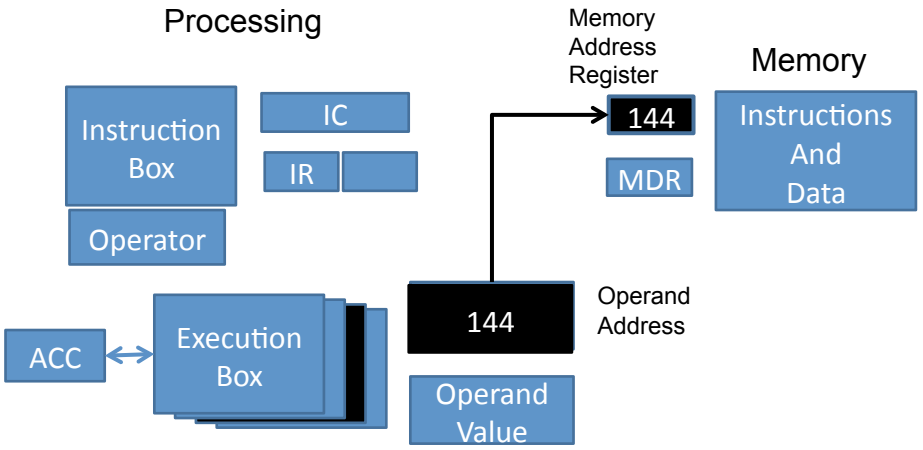
Von Neumann Architecture
Instruction Decode - Operand



Von Neumann Architecture
Instruction Decode - Operand



Von Neumann Architecture
Operand Fetch



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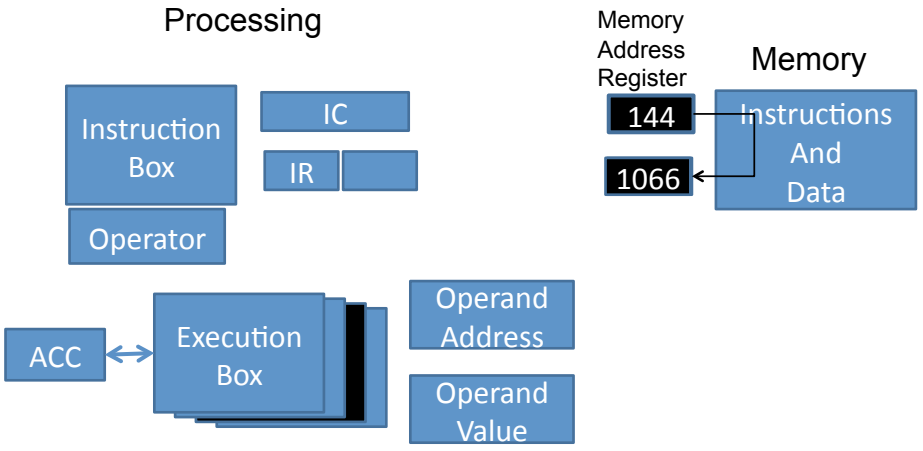
Operand Fetch



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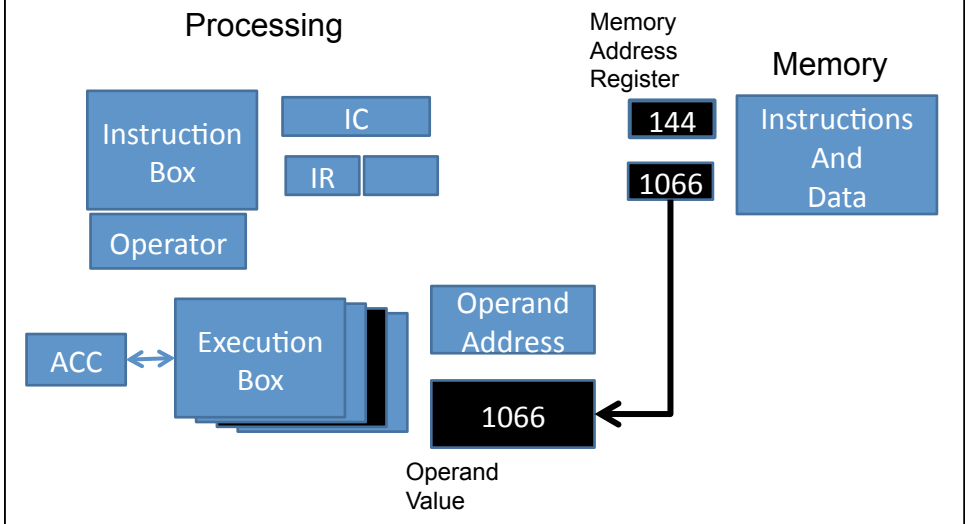
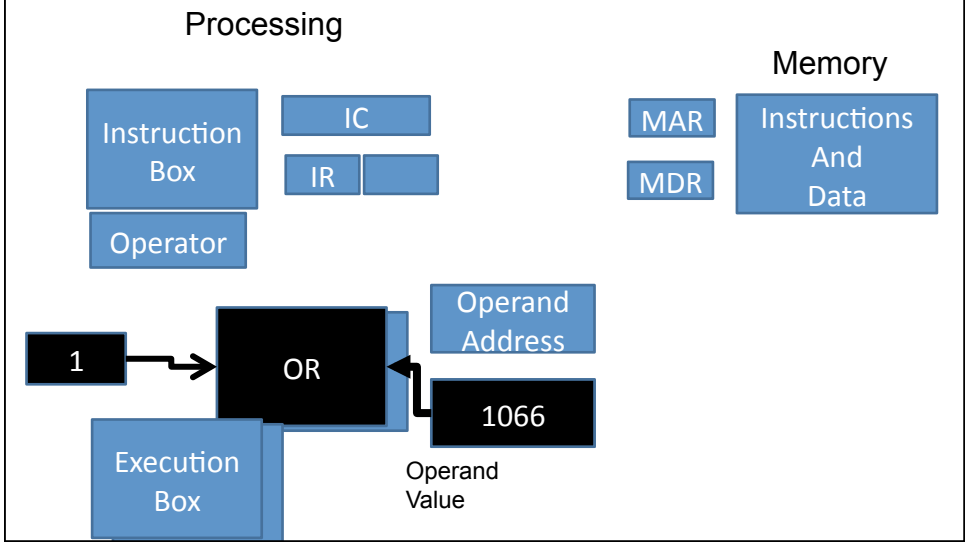
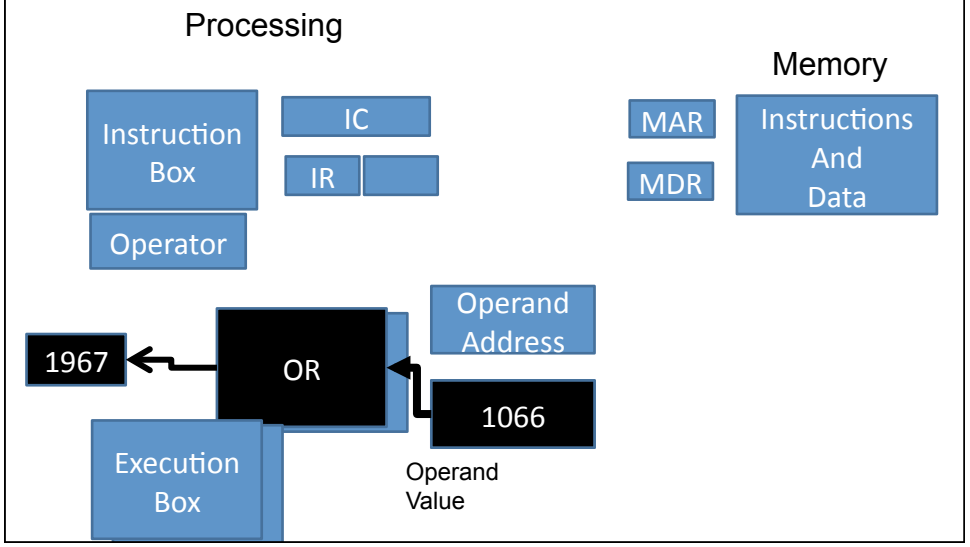
Operand Fetch



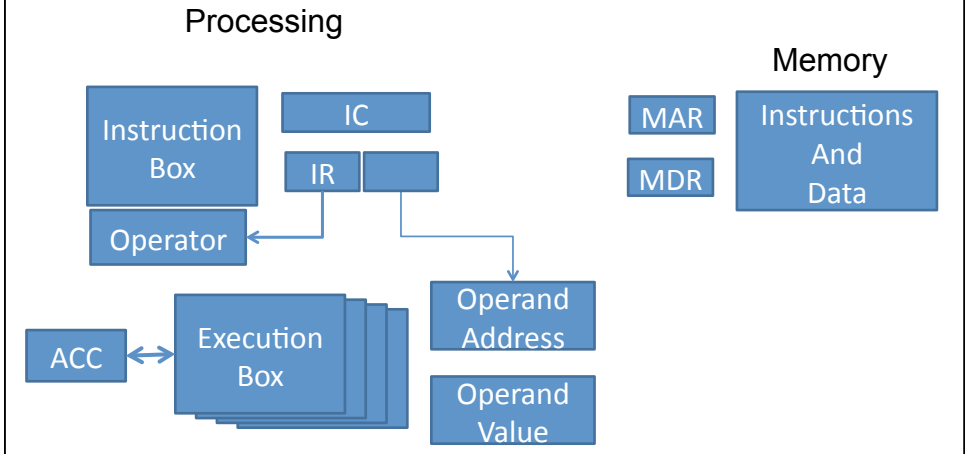
Von Neumann Architecture
Instruction Execution



Von Neumann Architecture
Instruction Execution



Von Neumann Architecture



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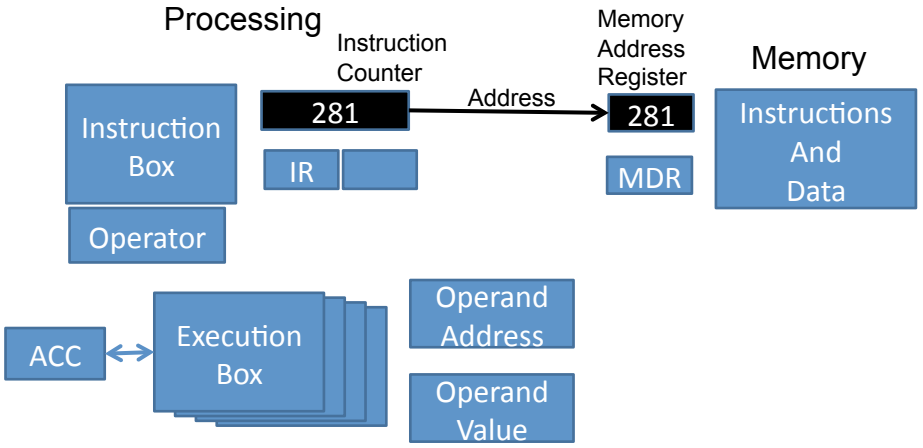
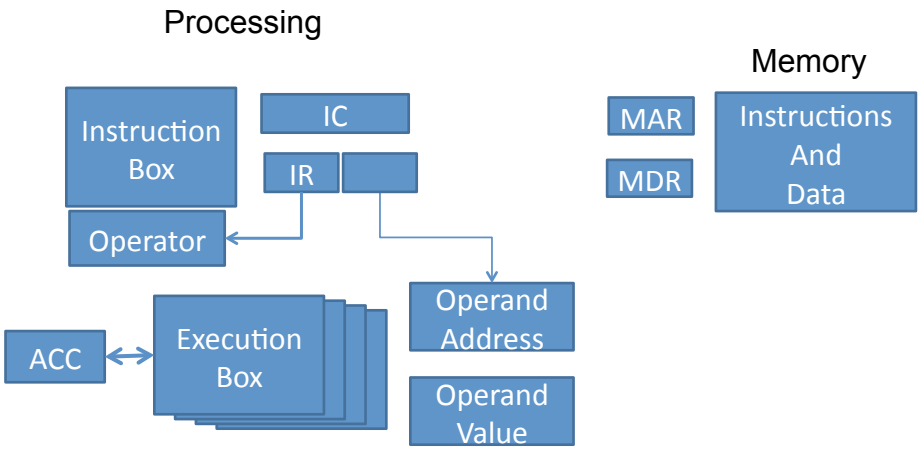
Instruction Fetch



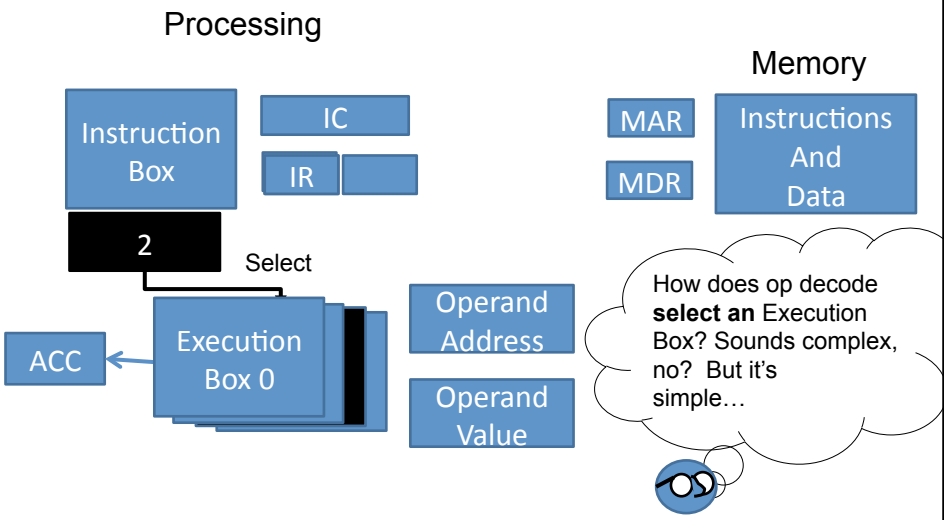
Von Neumann Architecture



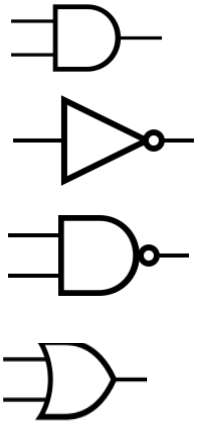
One Slightly Deeper Dive

- It's important to realize that the Processor is primarily composed of COMBINATIONAL (combinatoric) circuits, not SEQUENTIAL circuits
- You understand that the ALU devices are combinational – they produce the same input for a given output each time
- Let's look at operation select -- how do we actually select an e-box from an op code?

Von Neumann Architecture Instruction Decode – Op Code



Logic Gates

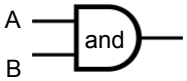


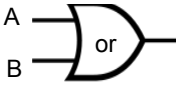
Integer Add
Integer Subtract
etcetera

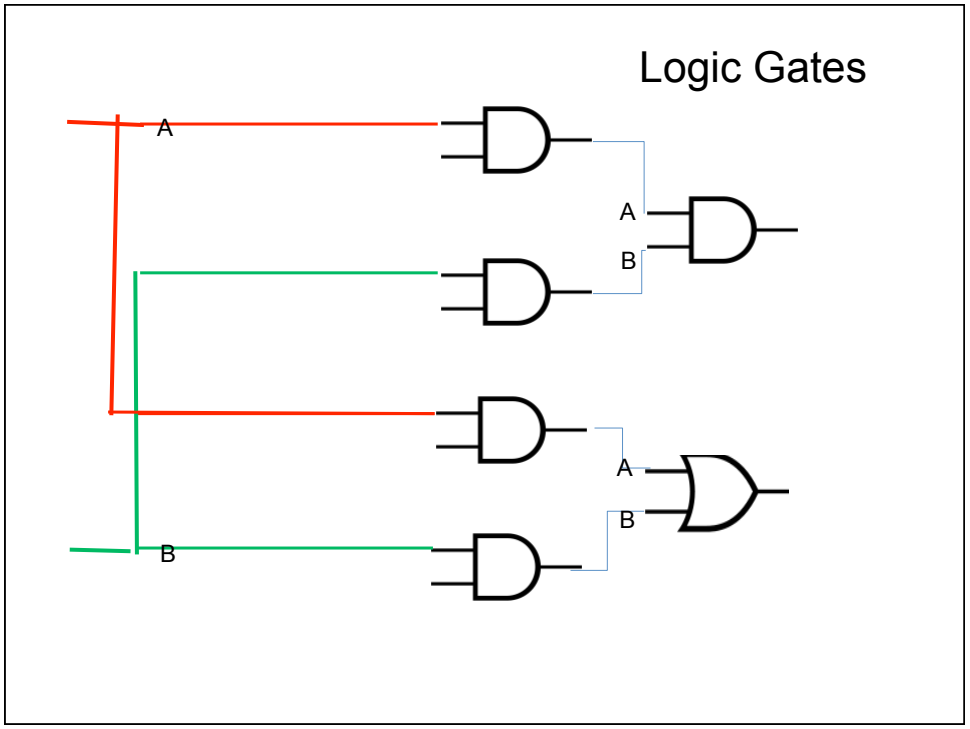
Logic Gates

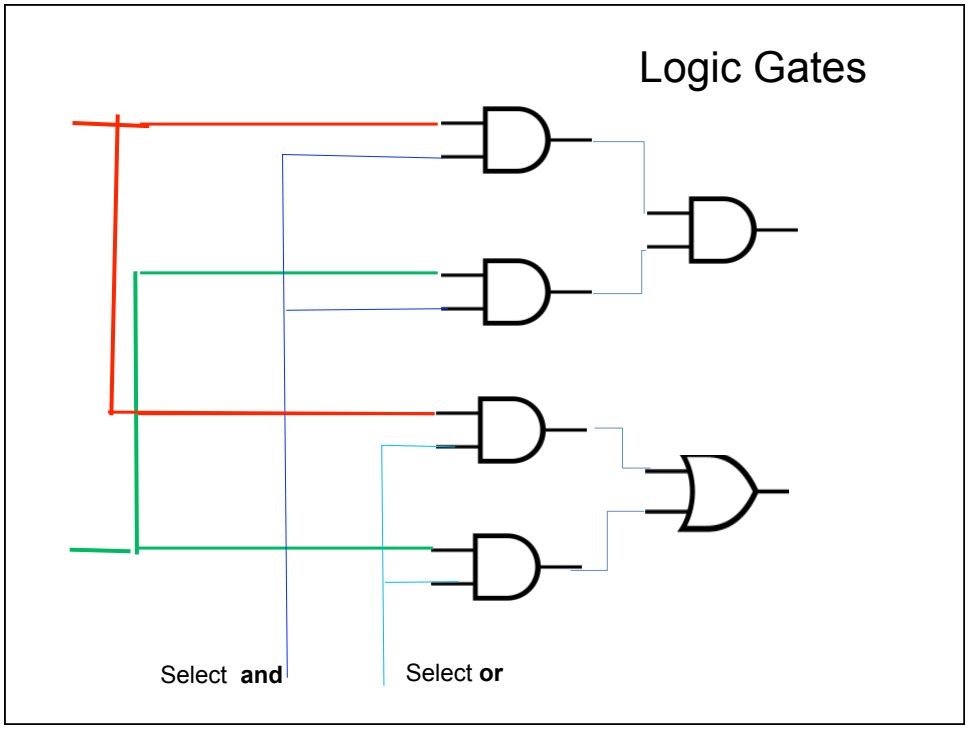
A

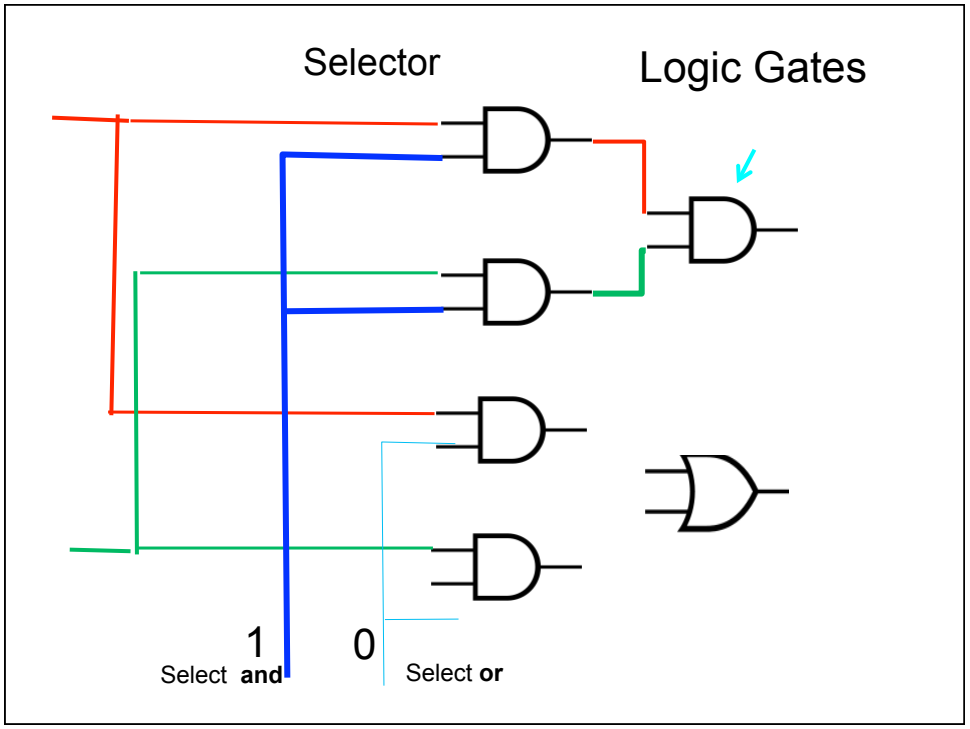
B

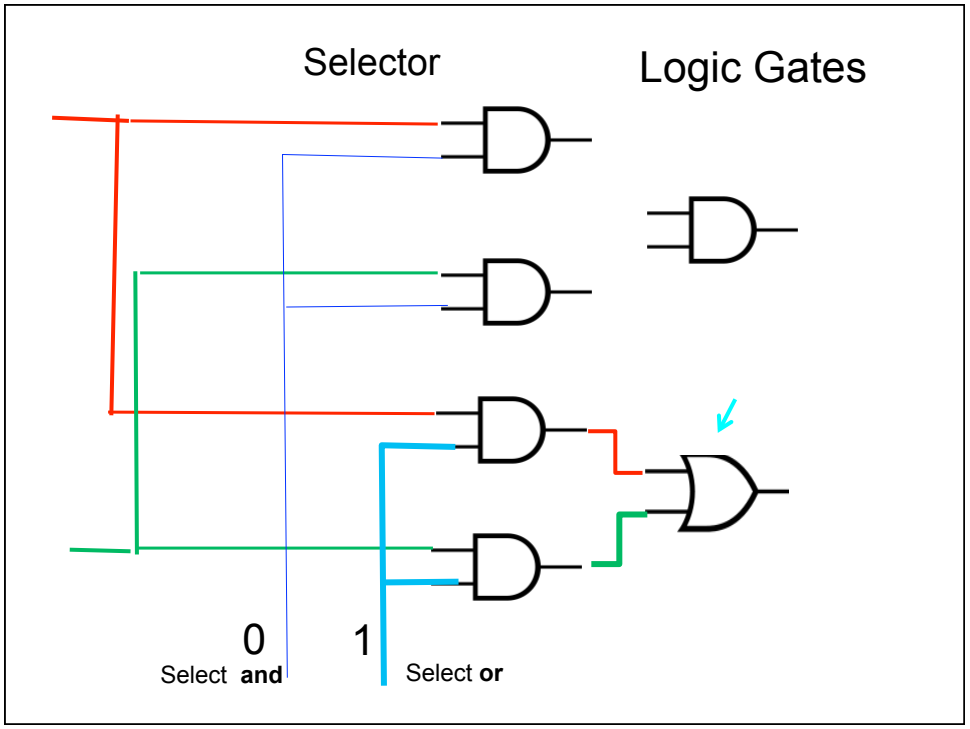





Logic Gates
A
A
B
A
B
B


Logic Gates
Select and
Select or

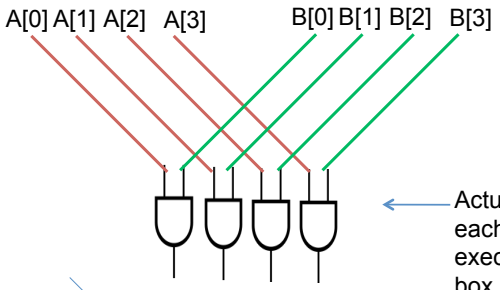

Selector
Logic Gates
1
Select and
0
Select or


Selector
Logic Gates
0
Select and
1
Select or

Address Decoder – convert op code to selection bits

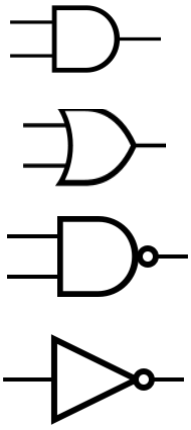
Input	Output	
0 0	1 0 0 0	nop
0 1	0 1 0 0	branch
1 0	0 0 1 0	or
1 1	0 0 0 1	and

If we have a 4-bit data width, we need 4 parallel logic gates and 8 wires

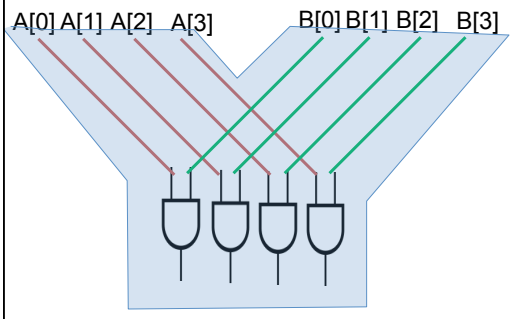


Actually, each execution box has a selector circuit of course

Logic Gates

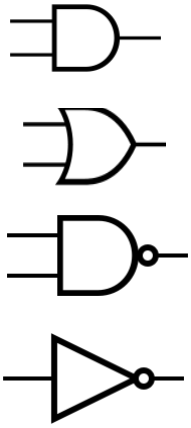


Execution Boxes are now
Called Arithmetic and Logical Units = ALUs



They are drawn as a "Y"
To indicate the fact they have
parallel inputs

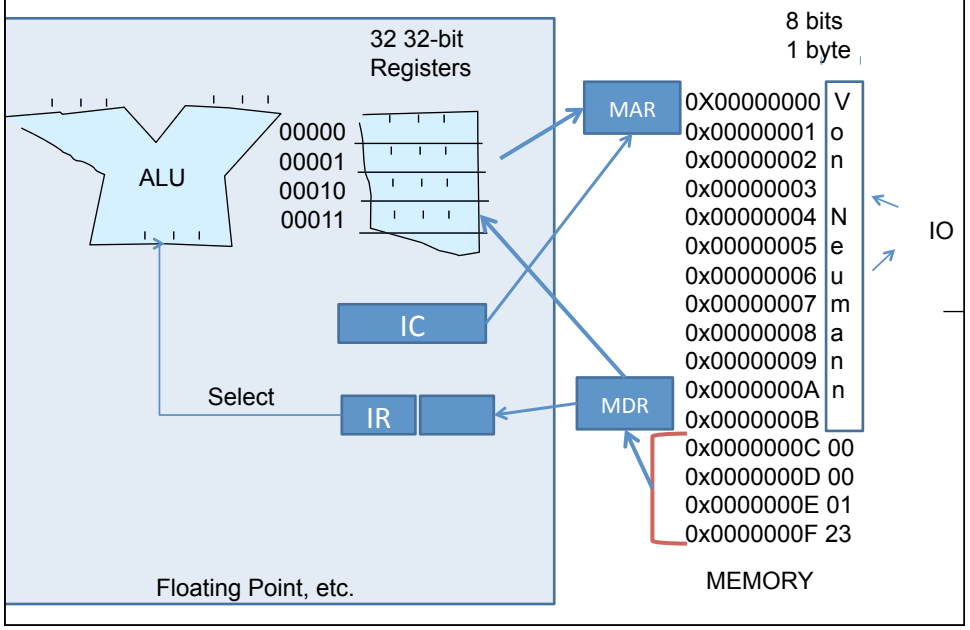
Logic Gates



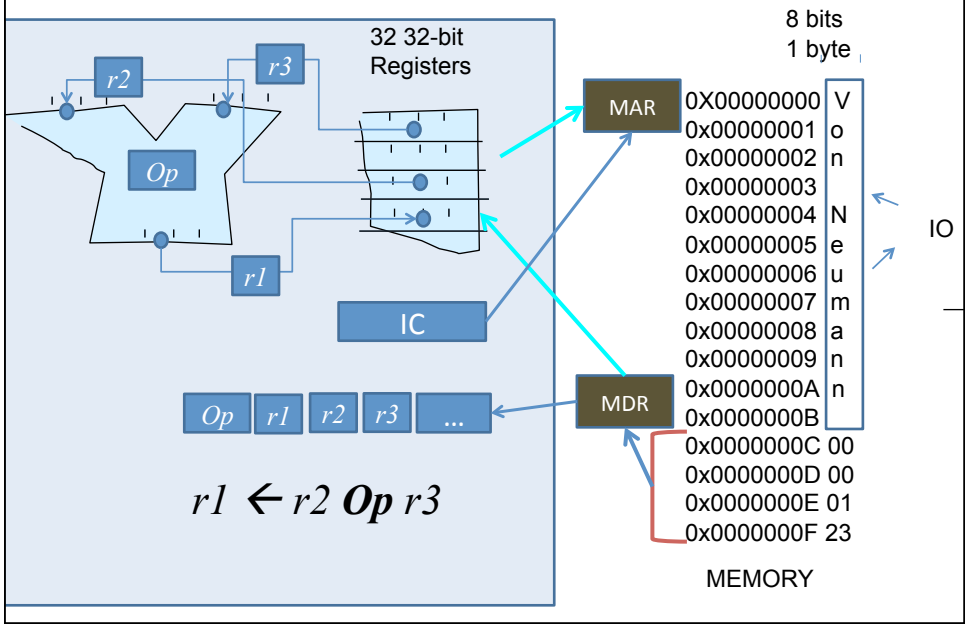
50 Years Later

- More memory = wider address registers)
- More operations = longer op codes
- Multiple accumulators = registers
- RISC:
  - Load and store are only memory ops
  - Other ops (and, or, add), are register to register
    - Register numbers replace memory addresses in instruction formats
- IO controlled by operating system rather than hardware
  - Protection schemes for operating system code

Same basic Von Neumann model



Multiple registers in instruction format



Many other optimizations in this and other machines …